AREA CODE 602 959-1000
EXT 218

NOT AFTER 5:00PM OR ON WEEKENDS

RAY BORHNERT MOTOROLA PHINIX ARIZ

CHUCK ALEXANDER

PM EVERY 6 MONTHS

COURSE NO. MDR

MOTOROLA DOCUMENT READER

STEP 1 - Red to BROWN
STEP 2 White to BROWN
Step 3 BK to US Yellow

AH - Remove shift
A7 - EJECT IN

MOTOROLA
COMMUNICATIONS and ELECTRONICS, INC.

MOTOROLA DOCUMENT READER

COURSE No. MDR

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PART I. - INTRODUCTION

The Motorola Document Reader is a data communication terminal used to transmit information to a receiving terminal where it may be stored, recorded, evaluated, processed and used for reporting, inventory, ordering, billing or innumerable other functions. The information is applied to the Document Reader by marking and/or punching a card, snap form or document in a coded language which is understood by the machine. The Document Reader in turn will transmit the information to the receiving business machine in any language that is desired by the receiving terminal.

This process of transferring data from one business machine to another business machine is a rapidly expanding area of electronics. The role of the electronics technician is now evolving into an area requiring a different viewpoint. Communication no longer means a voice transmitting a message by means of a modulated RF signal. The field of data communication requires that the technician gain an understanding of new concepts, new circuits and a new vocabulary.

Course No. MDR is presented to aid in the transition of producing a Data Communications Technician from a Two-Way Radio Technician. The information contained herein covers not only an analysis in depth of the Motorola Document Reader but also supplemental information on the circuits and devices used, the language codes encountered, the vocabulary used and the associated business machines. Every aspect and phase of the Document Reader's operation is covered.

Proficient servicing of the Motorola Document Reader by the technician may be accomplished by careful study and understanding of the material in Course No. MDR. The technician will derive great satisfaction and many benefits by acquiring this knowledge.

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MDR-II
TECHNICAL
TRAINING
DEPARTMENT

MOTOROLA DOCUMENT READER

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(INCLUDED AS PART OF THE TEST SET)

F. HAND TOOLS AS NEEDED

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TEXT

Figure 1. Motorola Document Reader with Data Set

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COURSE No. MDR

I. INTRODUCTION

A. MDR PURPOSE AND USE

The Motorola Document Reader (MDR) is a transmitting terminal designed to transmit information that is marked on documents to a receiving terminal that is either local or at a remote location. This could be compared to a radio in that the information or data modulates or adds intelligence to the carrier. However, there is no receiver in the MDR and there is no RF section or RF carrier.

Since the Document Reader is to be only a transmitting terminal, no provision is made for receiving information or data. Modulation is accomplished by recognizing information that is encoded on documents. When data is recognized, a change is produced in the "carrier" output. The carrier is simply voltage levels, a +12Vdc or a -12Vdc. The output is at either the one level or the other. Therefore, the transmission may be made on a two-wire line.

B. DATA TRANSMISSION

Data transmission stated simply would be communication between a source and a terminal. Whenever two people talk, they are transmitting data. However, the evolution of data transmission has progressed far beyond simple communication between two people.

1. History

   From talking to each other, data transmission progressed to hand signals to written materials to radio signals and television. The purpose in each case was to convey intelligence for greater distance with better efficiency. Data is now transmitted by means of encoding information on documents such as the familiar tab card (Refer to Figure 2) by either punching or marking the tab card.

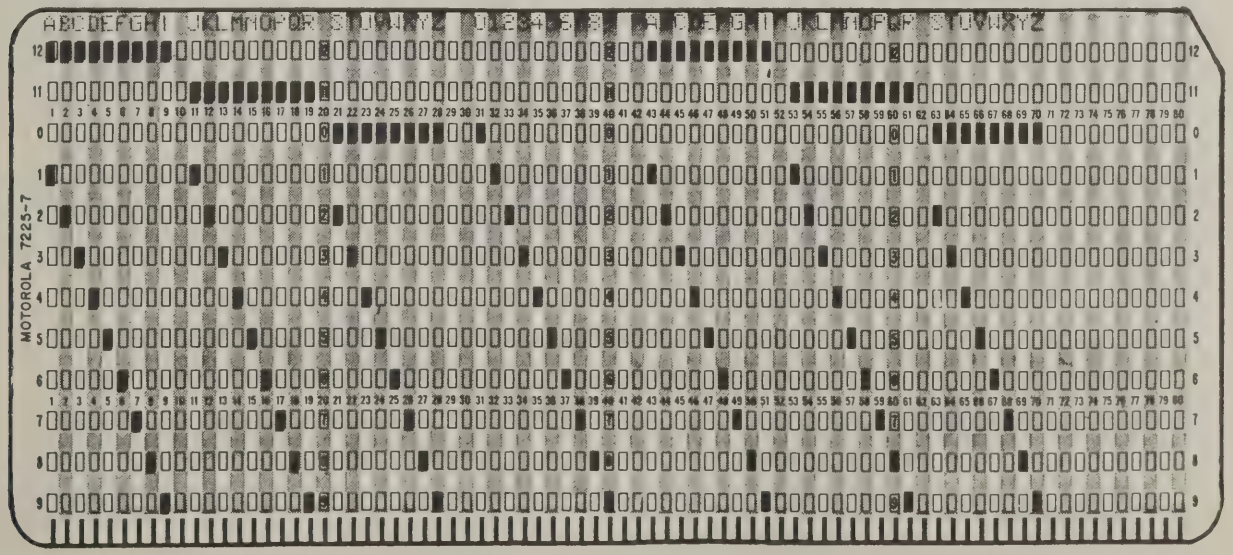


Figure 2. Punched Tab Card

2. MDR Data Transmission

The MDR takes encoded data from tab cards, page size documents or from snap forms. The data on any of these documents is limited to a 3-1/4" area along the edge. Data may be entered on the document by punching, marking, preprinting or any combination of the above.

The data is recognized by the use of phototransistors that are sensitive to changes in light levels caused by the entering of data on the documents. The changes in light levels are detected, decoded and encoded to produce the desired changes in the output of the Document Reader.

3. Transmission Media

Transmission of the coded signals may be made over a voice grade telephone line or a DC keyed line such as used with a teletypewriter. A wide bandwidth is not required since the signals are merely changes from one level to another.

C. ROLE OF THE TECHNICIAN

1. Installation

The technician will perform the complete installation of the MDR. This will include the unpacking, setup, connection to the interface equipment and a complete operational checkout. During this time, the technician should observe if any damage has occurred to the Document Reader during shipment.

2. Preventative Maintenance

Preventative maintenance checks will be performed twice a year by the technician. During the PM checks, close attention should be made to the condition of all moving parts, accumulation of dust and dirt in the sensing area, voltages within the tolerance range, that mechanical adjustments are proper and that all operations of the Document Reader are proper. All worn or defective parts should be replaced and any required adjustments should be made. A person of authority should be notified at the conclusion of the preventative maintenance check that the MDR is operating correctly.

3. Field Repair

When service is required (a reported service call) the technician will locate and replace the defective part. A problem isolated to a printed circuit board will be corrected by replacing the defective board. NO REPAIRS WILL BE MADE TO THE BOARD. The entire board will be returned for replacement. (An exception to this will be the power supply boards which will be repaired to the component level.) Other defective parts will be replaced from the technicians stock. All defective parts are to be returned for replacement (see Section VII - SERVICING AND REPAIR INFORMATION).

4. Warranty Service

Warranty replacement of defective parts will be limited to the warranty period unless the unit is under a Maintenance Agreement. In this case, replacement of all defective parts is included in the agreement. All defective parts must be returned to obtain replacement parts.

5. Factory Overhaul

In the event of serious damage to a Document Reader which is beyond the scope of field repair, the unit may be returned to Motorola Instrumentation Control, Inc., Phoenix, Arizona for a complete factory overhaul. Written permission and instruction should be obtained prior to shipment. A complete description of the damages should accompany the unit.

D. MOTOROLA BACKUP

To aid in maintaining the Motorola Document Reader at its maximum capabilities, Motorola provides service in three main areas. First, technical assistance is available from the factory to help solve any maintenance problems. This aid may be obtained by letter or by telephone. Information such as model number, serial number and symptom should be provided at the time of the request for aid.

Second, all parts of the Motorola Document Reader are available in stock at the factory. There need be no time delay in obtaining replacement parts. As soon as defective parts are received, new parts can be on the way to the technician.

Finally, in the event that the problem cannot be located by the technician, even with assistance by telephone or letter, the services of a Motorola Factory Field Service Representative may be obtained. Aid of the nature is limited to those extreme cases where other methods have not produced satisfactory results.

II. APPLICATIONS

A. TYPICAL USAGE

The Motorola concept of source-data entry is applicable to virtually any type of industrial, commercial, or service business. You will find the MDR anywhere data is to be recorded or processed by computer media such as magnetic tape, punched tape, key punches, or where it is transferred directly into a computer.

Data as entered on the source documents is translated into standard business machine languages, and then entered into an information processing system. This eliminates the need of keypunching and verifying the input media (tab cards).

Some typical applications are:

- Trouble Reporting

  In one major telephone company, the MDR speeds trouble reports on their way only seconds after they have been reported. The time span from "trouble reported" to "corrective action started" has been reduced from over 12 hours to 5 minutes with a considerable savings in cost over the system previously used.

- Purchasing Control

  At a large government electronics manufacturing facility, incoming Quality Assurance data is reported directly to the Purchasing department by means of an MDR. Patterns and trends concerning the condition of incoming goods are apparent within a short time period, thus supplying management with the information needed to make critical purchasing decisions.

- Inventory Control

  A large trucking firm is using a source document to itemize type and quantity of goods loaded into a van on the shipping dock. This information is then fed via an MDR into a computer to generate a manifest. Instant recording of goods movement is thus available.

- Service Reporting

  Service reports covering repair time, parts used, model numbers, serial numbers and location of equipment are marked on source documents and transmitted to a central location to be analyzed and evaluated.

- Utility Billings

  Utility companies, such as Water Companies, are using source documents for meter readings. Readings, taken by the meter man, are then sent to the billing department to prepare billing to the customer.

- Payroll

  Using special time cards as source documents, payrolls and payroll records can be coordinated in a central location, thus avoiding the need for several payroll departments.

B. INTERFACE EQUIPMENT

The Motorola Document Reader can interface to a wide variety of receiving devices. These receiving devices fall into two categories: modems and business machines.

Figure 3 shows a typical MDR system. Information recorded on tab cards, or page-size documents is fed into an MDR. The output of the MDR may be directly connected to a teletypewriter, tape punch, computer, magnetic tape recorder or keypunch, or the output may be transmitted via a data set or acoustic coupler to any of the above devices.

mdr system

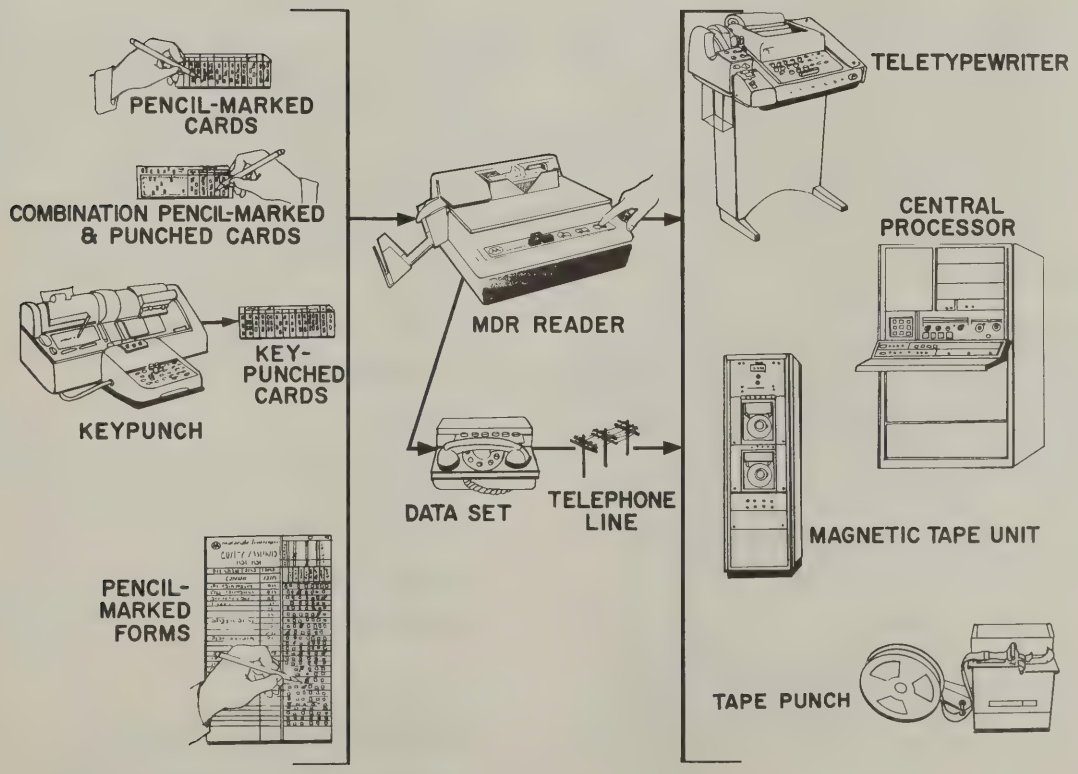


Figure 3. Typical MDR Systems

1. Modems

A Modem is a device that converts data, which is compatible with data-processing equipment, to a form that is compatible with transmission facilities (MOdulator DEModulator). Basically, a modem is used when data is to be transferred to a remote location. Data sets and acoustic couplers are the basic modem devices available.

a. Data Sets

In most applications, when data is to be transferred, the distance involved makes it impossible for the user to supply the facilities. When this occurs, the user normally requests the services of a communications facility. Telephone company data services use a hardwired data set and the regular dial-up telephone network to transmit the data electronically. The data set converts the binary data from the MDR into specific frequencies, making it suitable for transmission over voice-grade lines. In like manner, the data set at the receiving end converts the frequencies back to binary data which is suitable for digital equipment.

Various models of data sets exist, depending upon the degree of automation and transfer rates desired. Data sets are provided by private companies as well as by telephone companies.

b. Acoustic Couplers

Acoustic couplers are modems that convert binary data to tones and transmit the tones via a telephone handset using the regular dial-up telephone network. Since acoustic couplers are not capable of transferring data at higher speeds, they are limited in use to the MDR-1000 and 3000 Series Document Readers.

The MDR-3000 Series Document Reader includes a Motorola Acoustic Coupler.

2. Business Machines

Business machines are devices designed to accept and perform specific operations on incoming compatible data. With the MDR Document Reader capable of converting source data into a variety of business machine languages, direct interfacing between the Document Reader and various business machines is quite common. Some of the more common business machines used are: teletypewriter sets, magnetic tape units, and processors.

a. Teletypewriter Sets

The MDR Document Reader can interface directly to a teletypewriter set. Source documents as read are then printed on paper and/or punched on paper tape by the teletypewriter set.

The MDR Document Reader can, with permission of the local telephone company, operate in series with a local teletypewriter over telephone lines via a modem to a remote teletypewriter set.

b. Magnetic Tape Units

The MDR Document Reader can interface to a variety of magnetic tape units. A serial Document Reader or a parallel Document Reader can by used to transfer data in the form required by the magnetic tape unit.

c. Processors

The MDR Document Reader can interface to a variety of data processors. One of these is the Motorola MDP Data Processor. Information can be transferred in the form desired either by a serial or a parallel Document Reader as required by the processor.

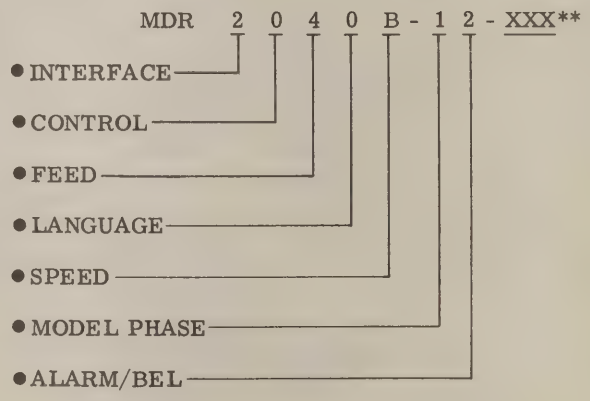
III. FEATURES

The Motorola Document Reader has an exceptional versatility through its multitude of features and options to enable adaptation to most customer requirements. These features and options which are presented in the following paragraphs indicate this versatility very aptly. However, special customer needs beyond those stated are also possible and it should be recognized that as requirements change, so will change occur in the features and options that are offered.

A. MODEL NUMBER SYSTEM

The model number of the MDR Document Reader provides the "key" to the optional features built into the machine. Part variations and options are identified by a combination of alphanumeric characters as outlined below:

MDR MODEL NUMBER*



*Refer to Model Number Table, Table 1, for existing model number configurations.

**Applies only to special units. Instruction Manual for special unit will be sent directly to customer.

MDR

INTERFACE	CONTROL	FEED	LANGUAGE	SPEED	MODEL PHASE	ALARM/BEL
9 Teletypewriter (Serial Data Transfer)	9	9	9	S	9	9
8 Parallel Data Transfer	8	8	8	J	8	8
7	7	7	7	H	7	7
6	6	6	6	G	6	6
5	5	5	5	F	5	5
4	4	4 Automatic with Eject Feature	4 Hollerith In Hollerith Out (Parallel Interface only)	E	4	4
3 Acoustic Coupled (Serial Data Transfer	3 Parallel Output	3	3 Hollerith IN PTTC/BCD Out	D	3	3
2 200 Series DATA-PHONE® (Serial Data Transfer)	2 Teletypewriter Interface	2	2 Hollerith In EBCDIC Out	C 10 characters /second	2	2 Hopper Empty Alarm Bel
1 100 Series DATA-PHONE® (Serial Data Transfer)	1 Attended Operation	1 Manual (only)	1 Hollerith In USASCII Out (numeric only characters)	B 70 characters /second	1 This digit currently used on all models.	1 Hopper Empty
0 Never Used	0 Unattended Operation	0 Never Used	0 Hollerith In USASCII Out (alphanumeric characters)	A 7 characters /second	0 Never Used	0 No Options

Table 1. Model Number Table

1. Interface

   The Interface digit identifies the type of device that is connected to the MDR output connector.

2. Control

   The Control digit identifies the type of operator control required before the machine will transfer information.

3. Feed

   The Feed digit identifies the type of feed (manual or automatic) the machine can perform.

4. Language

   The Language digit identifies the output language decoder boards.

5. Speed

   The Speed digit identifies the type of motor, drive pulleys, and bit oscillator board.

6. Model Phase

   The Model Phase digit identifies the production or model configuration.

7. Alarm/Bel

   The Alarm/Bel digit identifies the specific audible and visual types of alarm indications.

B. CAPABILITIES

The MDR Document Readers are capable of reading pencil-marked, key-punched, and preprinted data (or any combination of the three) appearing on standard or elongated tab cards, on forms, or on page-size documents of any practical length (Refer to Figure 4). The following paragraphs discuss the specific capabilities in detail.

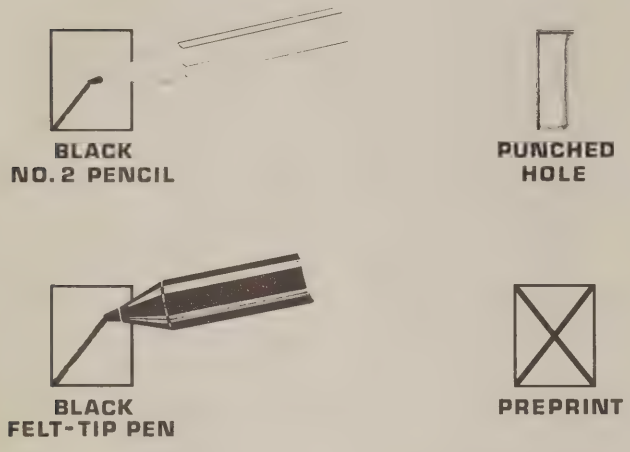


Figure 4. Methods of Entering Data on Documents

1. Reading Rates

Two reading speeds are standard:

- one for 40-column spacing on a standard size tab card, and
- one for 80-column spacing on a standard size tab card.

Table 2 lists the reading rates for the various model numbers.

Model Number Series	Reading Rate in cards/minute* 40-column	80-column
MDR-1000	6,8	3,4
MDR-2000	60	30
MDR-3000	6,8	3,4
MDR-8000 (low speed)	8	4
MDR-8000 (high speed)	60	30
MDR-9000	6,8	3,4

*Reading Rates given are minimum. Use of "End of Data Card Ejection" code can double reading rates given.

Table 2. Reading Rates

2. Data Transmission Rates

The reading rate of a document is directly limited by the speed of the receiving device; therefore, the specific interface device determines the maximum transmission rates for the various model numbers. (Refer to Table 3.)

Model Number Series	Transmission Rates
MDR-1000	0-30 characters/second
MDR-2000	0-120 characters/second
MDR-3000	0-30 characters/second
MDR-8000 (low speed)	0-150 characters/second
MDR-9000	0-30 characters/second

Table 3. Transmission Rates

Each character is comprised of a specific number of bits. High speed receiving devices require 10 bits per character, while low speed receiving devices vary from 9 to 11 bits per character.

3. Documents Accepted

The MDR will accept tab cards, page-size documents and forms. Documents can be up to 8-1/2 inches wide by any practical length as long as the reading area is confined to a 3-1/4 inch strip along the edge of the document (Refer to Figure 5).

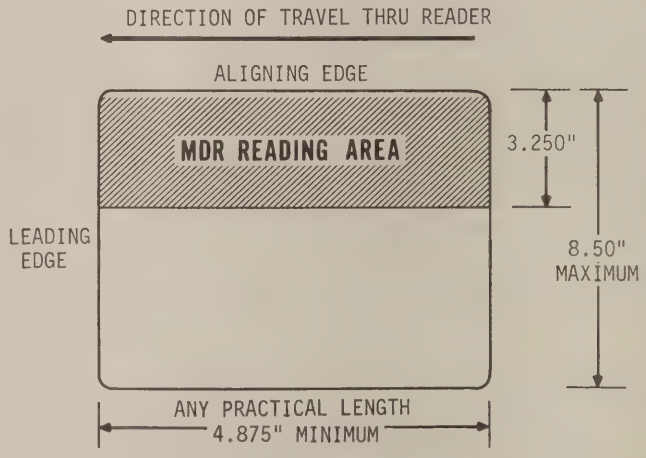


Figure 5. Reading Area

Within the reading area, the marking/punching positions are arranged in 12 evenly-spaced rows (Refer to Figure 6). This spacing is dictated by the position of the phototransistors within the read head.

Columns, on the other hand, are spaced as dictated by the application. Each data column must contain a format mark at the base of the column. The format mark is the control signal that informs the MDR that data is available.

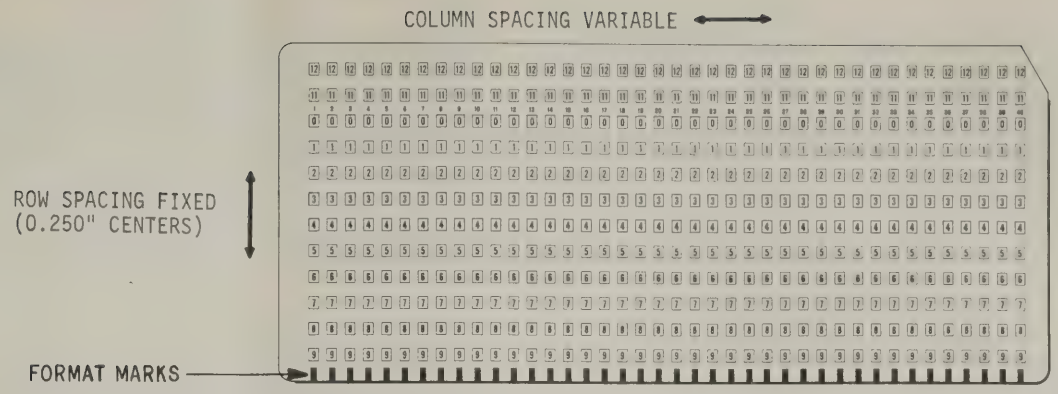


Figure 6. 40-Column Spaced Tab Card

a. Tab Cards (Figure 7)

The standard size tab card is 7-3/8 inches long, by 3-1/2 inches wide, by 0.007 inches thick. The most common formats in use are:

- 80-column, 1 or 2 Color Format - used for key-punch applications and preprinted data entry.
- 40-column, 2-Color Format - used for marked data entry, especially when considerable descriptive information is required for defining column usage.
- 40-column, 1-Color Format - used for marked data entry when little descriptive information is required for defining column usage.
- Combination Formats - used when cards are both keypunched and marked.

b. Page-Size Documents (Figure 7)

Page-size documents can be up to 8-1/2 inches wide by any practical length. The reading area for a page size document must be positioned as shown in Figure 5. Page formats are identical to tab card formats in all respects.

c. Forms

Snap-out or carbon forms can be either page-size or tab card-size. The reading area contains the same restrictions that apply to tab cards or page-size documents.

4. Program Codes

To identify and separate the data on each document, the Document Reader generates and transmits up to three automatic program codes for each document read. One or two program codes are generated as the document enters the read head; another is generated as the document exits the read head.

At the receiving device, these codes perform specific functions such as a line feed, carriage return, etc. Therefore, the person originating the document does not have to be familiar with the program codes required to identify and separate the data.

C. STANDARD ACCESSORIES

All MDR Document Readers are supplied with the following accessories:

- Power Cord (6-foot, 3-prong plug)
- Card Receiver
- Operator's Manual
- Dust Cover
- Test Cards

Various other items may be supplied but these are dependent upon the type of options incorporated in the unit (e.g., Interface Cable, Acoustic Coupler, Teletypewriter Interface Connector).

D. OPTIONS

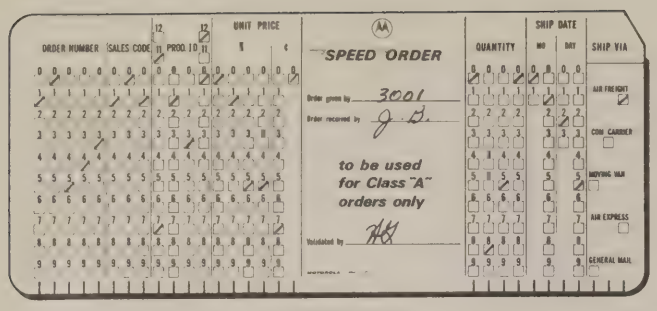
Various options are available as standard products, to be used with the Motorola Document Reader in order to conform with customer requirements. Some units will use no options, others will have one option, and a certain number will contain two or more options. The model number of the Document Reader will show which options are being used.

1. Automatic Feed

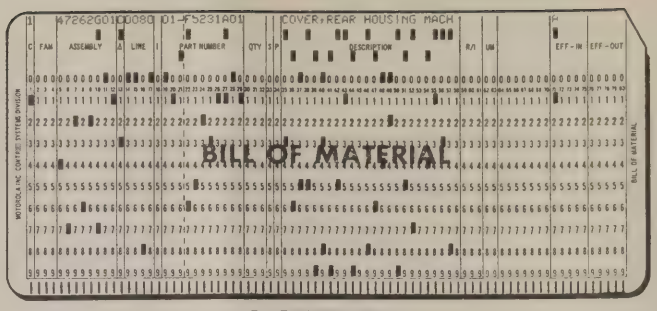
With this option, the Document Reader can store up to 250 tab cards for automatic feeding. Feeding can be initiated by a local operator (attended operation) or by a remote receiver (unattended operation). A special control function (Card Eject) is included with this option. The "Card Eject" function is a special Hollerith code ("12" and "11" rows marked) that causes the machine to increase its speed and to ignore all data on the card after detecting this code.

a. Attended Operation

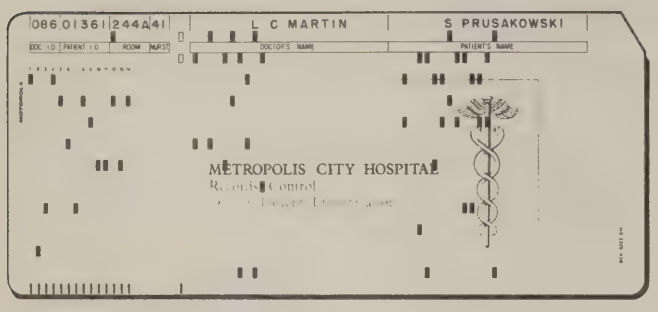
Automatic attended units require an operator to initiate the transmission of the data. This is accomplished by first establishing communication with the receiving device and then by starting the cards in the hopper to feed (depressing FEED switch). When the hopper



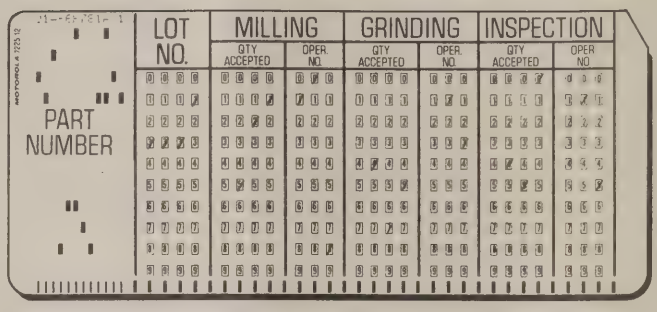
A. MARKED CARD



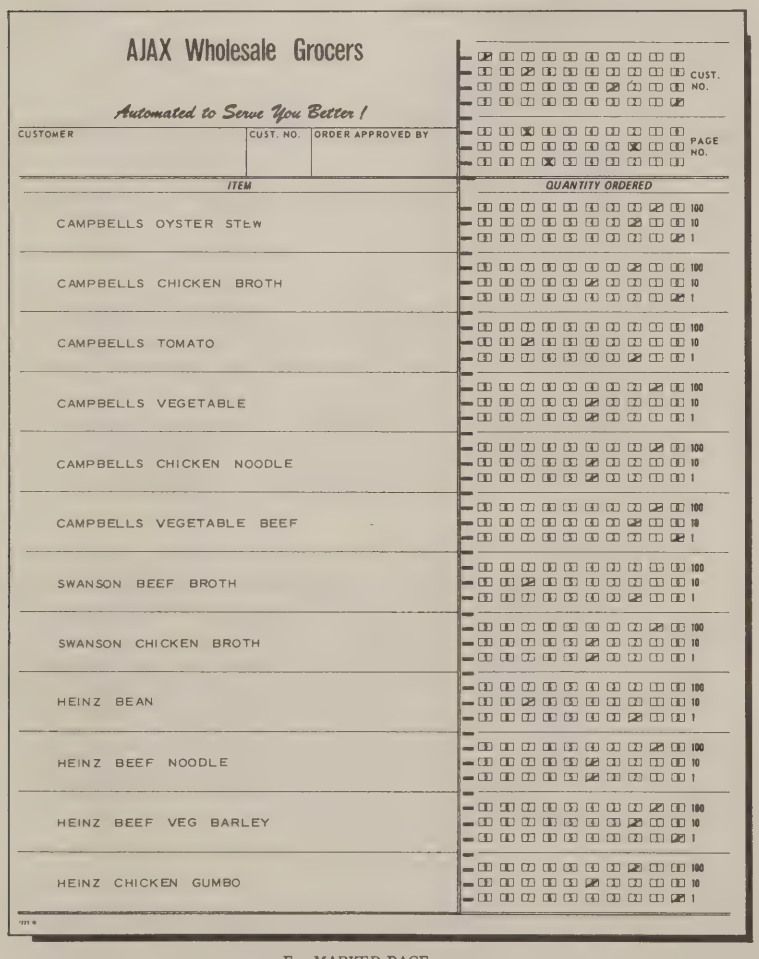
B. PUNCHED CARD



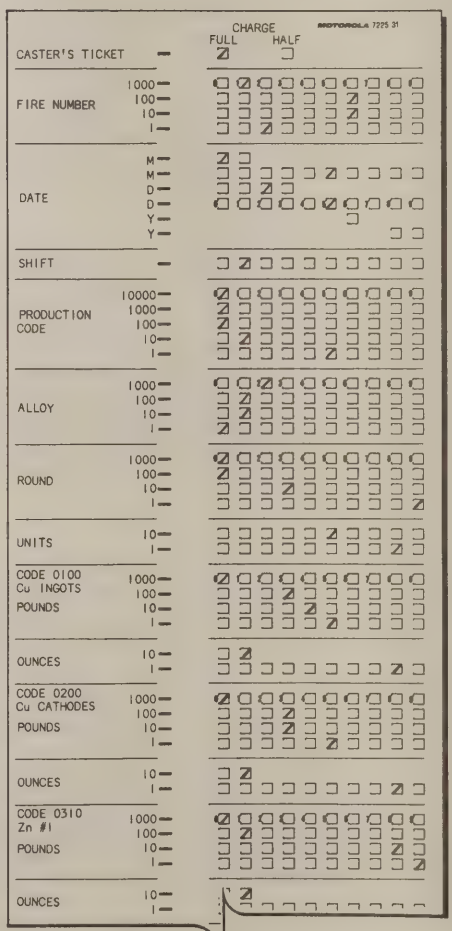
C. PUNCHED CARD



D. MARKED AND PUNCHED COMBINED



E. MARKED PAGE



F. SECTION OF 5" × 29" MARKED FORM

Figure 7. MDR Readable Document Formats

is empty, a red lamp (ALARM) on the operator's panel will light and an audible alarm will sound. The audible alarm may be silenced by a switch setting. The operator may then elect to either send more data by placing new cards into the hopper and depressing the FEED switch, or to terminate the connection with the receiving device.

b. Unattended Operation

Automatic unattended units are capable of operating as attended units or remote controlled units. When locally operated, the operator must establish communication with the receiving device. Once this has been accomplished, the MDR will automatically feed all cards in the hopper.

A red lamp (ALARM) on the operator's panel will light and an audible alarm will sound ten seconds after the hopper is empty or if a card fails to feed from the hopper. If no operator action is taken within 40 seconds, the unit will automatically turn off.

The unit may also be remotely controlled. A remote computer (or operator) may initiate a call to the Document Reader. The unit will automatically turn on, feed cards, and turn off 40 seconds after the last card has been fed.

Whenever the hopper is empty, a BEL code is transmitted to the receiving device. This code may be used to identify or separate incoming data.

Both the audible alarm and the automatic power shutdown may be disconnected by switch settings.

2. Output Languages

To be versatile, the Document Reader converts its input language into many standard business machine languages. Normally, a Hollerith code is used to mark or punch the input documents. The MDR receives the input data and, depending upon the type of decoders installed, it will output one of the following languages:

- USASCII - U. S. A. Standard Code for Information Interchange.
- EBCDIC - Extended Binary Coded Decimal Interchange Code
- PTTC/BCD - Paper Tape Transmission Code/Binary Coded Decimal
- Hollerith Code

a. USASCII Code

This language containing 128 output characters is used for exchanging information among processing systems, communications systems, and associated equipment. USASCII is a 7-bit coded character set plus a parity bit. The MDR normally decodes 85 alphanumeric characters. Using a special control code (SHIFT - "11" and "0" data rows marked), all 128 characters can be obtained. If desired, a 15 character, numeric only, USASCII code without shift may also be used.

b. EBCDIC Code

This coded character set is an 8-bit language with no provisions for parity. This language containing 256 output characters is normally used for magnetic tape information transfer. The MDR normally decodes 159 of these characters. Using a special control code (SHIFT- "11" and "0" data rows marked), all 256 characters can be obtained.

c. PTTC/BCD Code

This coded character set is a 6-bit language plus a parity bit. This language containing 64 output characters is normally used with typewriter applications. The MDR decodes all 64 characters. Using a special control code (SHIFT - "11" and "0" rows marked), an additional 8 characters (used for special control functions) can be obtained.

d. Hollerith Code

This coded character set is used with the MDR-8000 Series Document Readers for parallel transfer of information from the input cards directly to an interface device. No decoding is required. There are 4096 possible output codes available, although in reality only 50 to 70 characters are ever used.

IV. SUPPLEMENTAL INFORMATION

With the Motorola Document Reader, it is possible that there will be numerous terms, expressions and other associated equipment that will be unfamiliar. With this thought in mind, this section is devoted to discussing and explaining those items which are necessary for a complete understanding of the operation of the MDR.

A. DEFINITIONS

Associated with the MDR are a number of terms which need to be defined. This portion of Section IV will be concerned with items designated by words or letter combinations that are associated with the Document Reader.

1. Letter Identification

- CA (Request to Send) - This signal is generated by the Document Reader and supplied to the Data Set. It may be generated either upon receipt of a CC signal (Data Set Ready) from the Data Set or manually initiated from the FEED switch on the operator's panel. The signal condition is a change from a LOW level (-12Vdc) to a HIGH level (+12Vdc). It indicates to the Data Set that the MDR has data available.

- CB (Clear to Send) - The Data Set generates this signal and feeds it to the MDR when it has received CA (Request to Send) from the Document Reader. Upon receipt of CB from the Data Set, the MDR recognizes that conditions are acceptable for the transmitting of data. CB is always received from the Data Set in conjunction with another signal, either CF (Data Carrier Detector) or SB (Reverse Channel). The signal is recognized by a change of state from the LOW condition (-25Vdc to -3Vdc) to the HIGH condition (+3Vdc to +25Vdc).

- CC (Data Set Ready) - CC is a signal initiated by the Data Set to tell the Document Reader that it is operating and ready to receive data. It is only generated after the Data Terminal (MDR) has indicated that it is ready. When CC is received by the MDR, it will, in turn, generate CA (Request to Send). The active condition of the signal is a change from a LOW level (-25Vdc to -3Vdc) to a HIGH level (+3Vdc to +25Vdc).

- CD (Data Terminal Ready) - When the Motorola Document Reader is initially turned on, the DC terminal may be either HIGH or LOW. The HIGH level is the desired condition. There can be no communication between the MDR and the Data Set until CD is at the HIGH level (+12Vdc). If CD is HIGH when the set is turned on, then the Document Reader and the Data Set are ready to communicate. If conditions are such that CD is LOW, a circuit contained in the Document Reader will automatically cause CD to go HIGH after a time delay of 40 seconds. The CD signal is the first of the communicating or "handshaking" signals between the Motorola Document Reader and the Data Set.

- CF (Data Carrier Detector) - The CF signal is similar to, and may be used in place of, the CC (Data Set Ready) signal. Like the CC, it would only be generated upon receipt of CD (Data Terminal Ready) from the MDR. And, like CC, when CF is received by the Document Reader, CA (Request to Send) will be generated by the MDR. The levels for CF will be the same as for CC (-25Vdc to -3Vdc for LOW and +3Vdc to +25Vdc for HIGH). The difference between CC and CF lies in the fact that CC is generated by the Data Set at the Document Reader site, while CF is generated by the Data Set at the terminal end of the telephone lines and passed through the Data Set at the Document Reader to the MDR.

- SB (Reverse Channel) - The last signal in the "handshaking" routine between the Document Reader and the Data Set is SB (Reverse Channel). It essentially arrives at the MDR at the same time as CB (Clear to Send). At this time, the Document Reader, the Data Set connected to the MDR, and the Data Set and Data Terminal at the terminal end are ready to transfer data. The Motorola Document Reader will now send data. When SB (Reverse channel) is established, the change of state is from a LOW level (-25Vdc to -3Vdc) to a HIGH level (+3Vdc to +25Vdc).

- L. E. (Leading Edge) - The term L. E. (Leading Edge) can refer to two interrelated items. One is the leading edge of a card or document; the second is the change in state of the signal level when the leading edge of a document enters the L. E. sensing area. L. E. (Leading Edge) will be used interchangeably for both the leading edge of the document and the leading edge signal. The signal will be a change in level from a LOW level (0. 0Vdc to 0. 5Vdc) to HIGH level (4. 5Vdc to 5. 0Vdc).

- T. E. (Trailing Edge) - Like the L. E. (Leading Edge), a double usage will be associated with the letter code T. E. (Trailing Edge). It will refer to both the trailing edge of the card and to the signal obtained when the LEADING EDGE of the card enters the T. E. sensing area. Notice that it is again the leading edge of the card that is causing the change of signal condition. The signal will be a change in level from a LOW (0. 0Vdc to 0. 5Vdc) to a HIGH (4. 5Vdc to 5. 0Vdc) condition.

2. Word Identification

- Format Clock - This refers to the signal created by sensing the presence of special timing marks (format marks) that are preprinted along the bottom or "9" side of a card or document. The signal is a transition from a LOW level (0. 0Vdc to 0. 5Vdc) to a HIGH level (4. 5Vdc to 5. 0Vdc) lasting for the duration of the width of the timing mark and occurring every time a timing mark is recognized.

- Gated Clock (Window) - After the Clock signal is recognized, it is processed through circuitry and becomes the Gated Clock (Window). The WINDOW means that during the time of this signal, the "window" is open to look for data. The Gated Clock (Window) signal is a transition from a LOW level (0. 0 Vdc to 0. 5Vdc) to a HIGH level (4. 5Vdc to 5. 0Vdc) and back to a LOW level again. Every time a Format Clock signal is generated, a Gated Clock (Window) is also generated.

- Gated Clock (Logic) - At the same time that a Gated Clock (Window) is being generated as a transition from a LOW level to a HIGH level and back to LOW again, a Gated Clock (Logic) signal is generated that is exactly the opposite. That is, this signal will be from a HIGH level to a LOW level and back again to a HIGH level. This signal is used in an alarm circuit for the purpose of recognizing a malfunction.

- Pre-Card - The term pre-card will be used in conjunction with preset codes that are generated internally in the circuitry of the Document Reader. The codes, known as PROGRAM CODES, are used to perform various

functions that are desired by the user. Two such codes are available as pre-card program codes and are known as pre-card program code #1 and pre-card program code #2. Both codes are initiated by the L. E. (Leading Edge) of the card entering the sensing area. The signals thus generated are recognized by a change in state from a HIGH level (4. 5Vdc to 5. 0Vdc) to a LOW level (0. 0 Vdc to 0. 5Vdc) condition.

- Post-Card - The term post-card is again used in conjunction with a program code. Several functions are available to be used as a post-card program code. The code is activated as the T. E. (Trailing Edge) of the card leaves the sensing area. The signal thus generated is a change from a HIGH level (4. 5Vdc to 5. 0Vdc) to a LOW level (0. 0 Vdc to 0. 5Vdc) condition.

- Card Eject - Eject is a term used to identify a function which is "End of Data Command Ejection." This function is used to increase thruput by increasing the speed of transport of the cards once all pertinent data has been retrieved. By marking a special code at the end of the data area, the card can be rapidly removed from the sensing area, and thus shortens the time interval before more data is available. The function is activated by marking a special code on the cards (a mark in rows "12" and "11"). The signal is recognized by a change from a HIGH level (4. 5Vdc to 5. 0Vdc) to a LOW level (0. 0Vdc to 0. 5Vdc) condition.

- BEL - BEL refers to the bell character. The character is used to call for human attention. It may activate bells, lights, etc. BEL is used in the Document Reader to indicate that the last card has left the sensing area and a new card has not been fed for 1. 2 seconds.

- Shift Register - A shift register is a device capable of storing a specified amount of data and then moving the data to the right or left. In the Document Reader, a full character is stored in the register as parallel information and then is shifted to the right to provide an output as sequential or serial data.

- BIT - A contraction of "binary digit", this term is used to denote the smallest unit of information in a binary system. A bit may be either a one or a zero.

- Parity - A binary digit appended to an array of bits to make the sum of all the bits always odd or always even. In the Document Reader it is possible to have ODD, EVEN or NO parity.

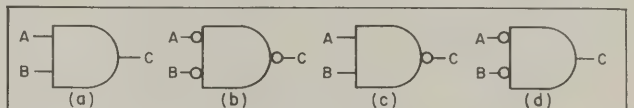
B. LOGIC THEORY

The best possible means of attaining full understanding of the circuits and operation of instruments used in the data acquisition field is through the use of LOGIC SYMBOLS arranged in LOGIC CIRCUITS. Therefore, at this time a basic description of the symbols used in the Document Reader and their theory of operation will serve to facilitate understanding of the Logic Circuits to be presented during the functional analysis of the MDR. Remember that this will be a basic description and further investigation and study of logic symbols and circuits may prove helpful.

1. AND Circuit

   a. Symbol

   One of the more commonly used symbols in logic circuits is the AND circuit or AND gate. There are several variations of this circuit as shown in Figure 8.



INPUTS		OUTPUT
A	B	C
L	L	L
L	H	L
H	L	L
H	H	H

INPUTS		OUTPUT
A	B	C
L	L	L
L	H	H
H	L	H
H	H	H

INPUTS		OUTPUT
A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

INPUTS		OUTPUT
A	B	C
L	L	H
L	H	L
H	L	L
H	H	L

Figure 8. AND Gate Symbols

All symbols, however, are presenting the same basic fact. This fact is that an input at A and an input at B is required in order to achieve the designated output. The only difference is in what level of input is required and what level of output is desired. In Figures 8 (a) and (b), the level required on the inputs is identical with the level attained on the output. Figures 8 (c) and (d) show the levels required on the inputs to produce an opposite level on the output. The latter symbols represent AND circuits with inverted outputs.

In each instance, there is one, and only one, set of circumstances in which the required output is obtained. Referring to Figure 8 again, under each symbol is a Truth Table. that provides a tabulation of all the possible combinations that the circuit is capable of producing. The L in the table refers to a LOW level signal and the H refers to a HIGH level signal. The term HIGH level means the more positive of the two levels at any one particular gate and the term LOW level means the less positive of two levels. A LOW level input or output on the symbol is indicated by the small circle in conjunction with the lead (see Figure 8 (b)).

   b. Theory

   A typical AND circuit is shown in Figure 9.

   As can be seen from the schematic, a HIGH level signal is needed at input A and B in order to produce a HIGH level output at C. If this condition is not observed, the output will not be a HIGH level signal. Therefore,

this circuit conforms to all the requirements for an AND circuit.

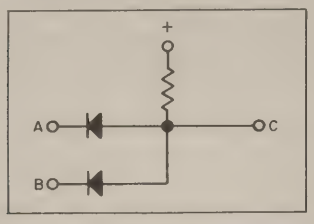
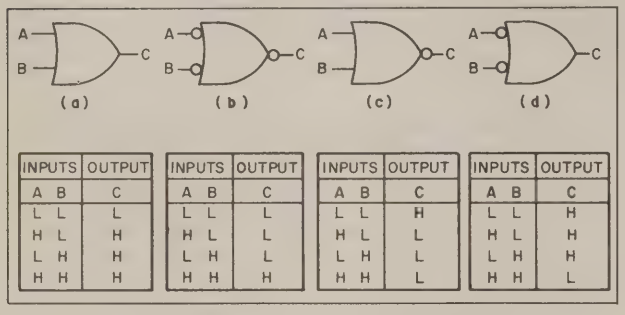


Figure 9. Typical AND Circuit

2. OR Circuit

a. Symbol

Figure 10 shows variations of the OR circuit. Like the AND gate, extensive use of the OR gate is found in logic circuits.



INPUTS	OUTPUT
A B	C
L L	L
H L	H
L H	H
H H	H

INPUTS	OUTPUT
A B	C
L L	L
H L	L
L H	L
H H	H

INPUTS	OUTPUT
A B	C
L L	H
H L	L
L H	L
H H	L

INPUTS	OUTPUT
A B	C
L L	H
H L	H
L H	H
H H	L

Figure 10. OR Gate Symbols

And like the AND gate, all the symbols represent the same basic fact. That is, an input at A or an input at B produces the desired output. Multiple inputs may be used and in each case, having either A or B or C, etc. at the indicated level will produce the desired output.

As can be seen from the truth tables, there is one, and only one, set of circumstances in which the desired output is not obtained. In this respect, the AND gate and the OR gate are exact opposites.

b. Theory

A schematic of a typical OR gate is shown in Figure 11.

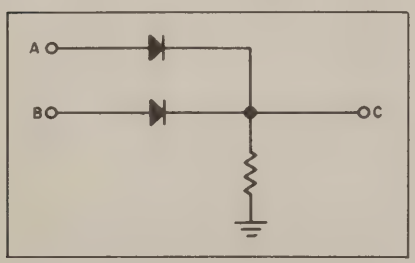


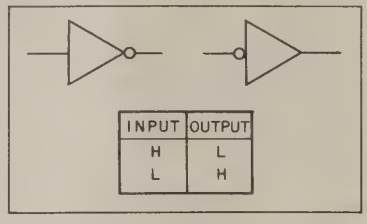
Figure 11. Typical OR Circuit

As can be seen from the circuit, a HIGH level input at A or a HIGH level input at B or a HIGH level input on both A and B will result in a HIGH level output at C. Therefore, if any of these conditions are present, the output will be as required, a HIGH level output.

3. INVERTER Circuit

a. Symbol

The inverter circuit does exactly what its name implies. It inverts the level of signal input. Certain circuits require a specific level of input. If the output of the preceding active circuit is not of the correct level, an inverter circuit is inserted between the two active circuits. The symbols for the inverter circuit are shown in Figure 12.



INPUT	OUTPUT
H	L
L	H

Figure 12. Inverter Symbols

As can be seen from the truth table, the input and the output of an inverter are the reverse of each other.

b. Theory

A typical inverter circuit is shown in Figure 13.

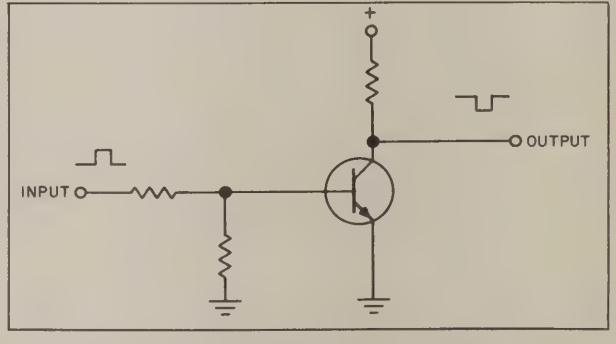


Figure 13. Typical Inverter Circuit

If a LOW level signal is applied to the circuit, the transistor is in a non-conducting state. At this time the output would be approximately supply voltage or at a HIGH level (the reverse of the input level). However, as soon as the input goes HIGH (more positive), the transistor becomes forward biased and conducts heavily. The collector of the transistor, and hence the output, approaches ground potential or goes LOW. The output will stay LOW as long as the input stays high. Therefore the input and output

are inverse to each other and the circuit is an inverter circuit.

The inverter circuitry represented by the symbol may consist of one or more stages and may or may not produce a gain.

A variation of the inverter is shown in Figure 14 and is the amplifier.

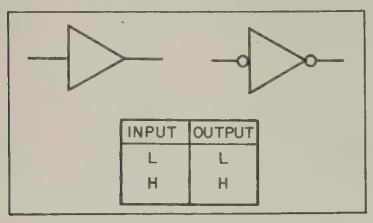


Figure 14. Amplifier Symbol

Most statements pertaining to the inverter also apply to the amplifier except for one factor. The input and output of the amplifier are not the inverse of each other. Thus, an amplifier stage which did not have inversion between input and output would be called an amplifier while a stage that did produce an inversion between input and output would more correctly be called an inverter.

4. FLIP-FLOP Circuits

There are many circuits which may be grouped under the designation FLIP-FLOP. Only the specific circuits used in the Motorola Document Reader will be discussed in this section.

a. Symbols

Figure 15 shows the symbols used to indicate the various types of FLIP-FLOP circuits.

All of the symbols may be used. However, the most commonly used is the lower example of (a), (b) and (c) of Figure 15.

b. RS Flip-Flop (Bistable Multivibrator) Theory

The flip-flop is a device which stores a single bit of information. It has three possible inputs: Set (S), clear or reset (C) and toggle or trigger (T). However, in the MDR use of the RS Flip-Flop, no trigger (T) input is used.

A flip-flop has two possible outputs, identified as the "1" output and the "0" output. The "1" output is shown at either the top or the right of the symbol and the "0" output is at the bottom, or left of the logic symbol. The "1" and "0" designations are entirely independent of the level of the output at any given time. A HIGH or "1" is stored in the flip-flop when the "1" output is HIGH and the "0" output is LOW. A LOW or "0" is stored in the flip-flop when the above condition is reversed.

The flip-flop assumes the HIGH or "1" state when a LOW signal appears at the "S" input, regardless of the original state. It assumes the LOW or "0" state when a LOW signal appears at the "C" input, regardless of the original state. If a LOW signal appears at the T input when it is used, the flip-flop reverses itself. There are several possible variations to normal flip-flop operations which depend upon the response of the device when input signals are applied to more than one input simultaneously.

Figure 16 shows a typical RS flip-flop circuit such as is found in the Motorola Document Reader.

Normally, a clear input is supplied to all flip-flop circuits during initial power application so that all of the circuits are in the clear (or reset) mode when operation begins. In the circuit shown, a negative pulse at the clear input causes transistor Q2 to be cut off. The positive voltage via resistor R2 is applied to the base of Q1 causing it to conduct. In so doing, the collector of Q1 ap-

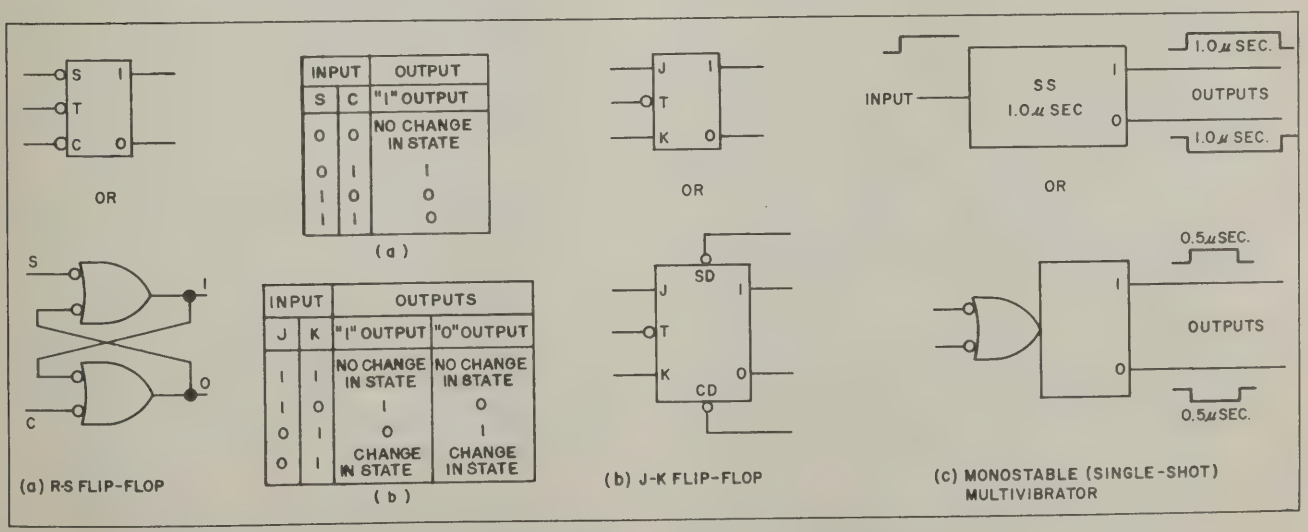


Figure 15. Flip-Flop Symbols

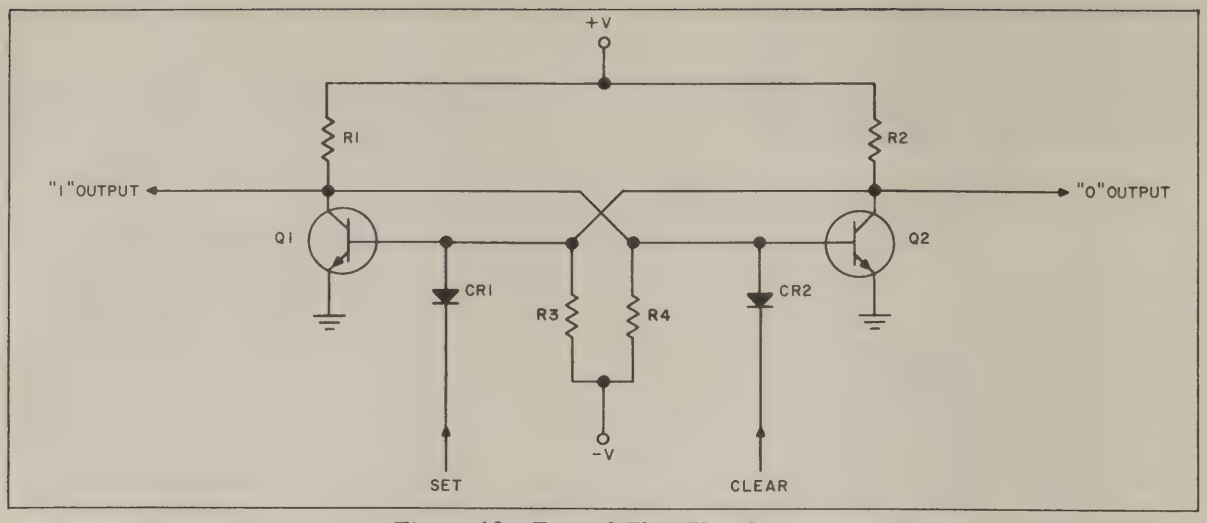


Figure 16. Typical Flip-Flop Circuit

proaches the ground potential at its emitter; this ground potential is applied to the base of transistor Q2 holding it cut off. Flip-flop output "0" is positive or HIGH.

When a negative pulse is applied at the set input of the flip-flop, transistor Q1 is cut off and its collector potential rises towards the positive supply voltage. At the same time this positive collector potential applied to the base of transistor Q2 causes the transistor to conduct. The collector of conducting transistor Q2 swings toward the ground potential of its emitter; this ground potential applied to the base of transistor Q1 holds Q1 in the cut off mode. Flip-flop output "1" is positive or HIGH.

In certain circuits, for instance the Data Registers, both outputs are utilized at the same time. That is, the "1" output goes HIGH or positive and at the same time, the "0" output goes LOW or less positive. Then both outputs are applied to inputs to perform a specific function. Thus a single input provides two outputs with which to perform operations.

c. JK Flip-Flop (Bistable Multivibrator) Theory

The JK flip-flop, like the RS flip-flop, has a "1" and "0" output, a set (J) input, a clear (K) input and a toggle or trigger (T) input. Unlike the RS flip-flop, however, the toggle (T) is always used. Two more inputs are available. These are the Sd (direct set) and the Cd (direct clear).

The Sd activating input is one that drives the flip-flop to the HIGH or "1" state regardless of the inputs at J, K or T. The Cd activating input is one that drives the flip-flop to the LOW or "0" state regardless of the inputs at J, K, or T.

The JK flip-flops are used extensively in control logic circuits. Besides being used as a single circuit to perform an operation, they may be joined in series with other JK flip-flops for the purpose of performing a more complex function.

d. Single-Shot (Monostable Multivibrator) Circuit Theory

The single-shot is exactly what its name implies. Upon receipt of an input pulse, the circuit changes from its quiescent state to its active state, remains for a time period determined by an R-C network in the single-shot and relaxes back into its quiescent state again, remaining there until the next input pulse. The output shape, amplitude, duration and polarity are determined by the circuit characteristics of the single-shot rather than by the input and may be shown either inside or outside the symbol (Refer to Figure 15 (c)). The outputs of a single-shot are complementary.

Figure 17 shows a typical single-shot circuit. In the stable state, current through resistor R2 holds transistor Q2 in conduction. Capacitor C1 is charged to a voltage slightly less than the supply voltage. The charge path for the capacitor is through resistor R1, the base-emitter junction of conducting transistor Q2, resistor R6 and the power supply.

The circuit is triggered when a positive pulse is applied at the input through diode CR1 to the base of transistor Q1. Transistor Q1 begins to conduct and its collector potential swings negative. This negative-going voltage is coupled to the base of transistor Q2, decreasing its forward bias and driving it out of saturation. The collector of transistor Q2 starts to go positive. This positive swing is coupled via capacitor C2 and resistor R3 to the base of transistor Q1 thereby increasing its forward bias and allowing it to conduct more heavily. This regenerative action results in a rapid change in the state of both transistors, Q1 going into saturation

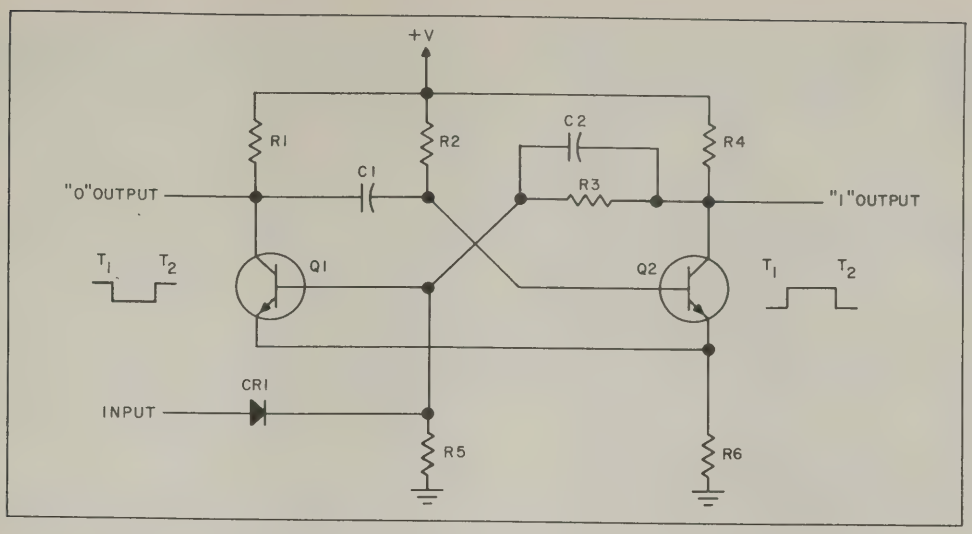


Figure 17. Typical Single-Shot (Monostable Multivibrator) Circuit

and Q2 into cut-off. As capacitor C1 discharges through the collector-emitter junction of transistor Q1, resistor R6, the power supply and resistor R2, the base of transistor Q2 becomes less negative. Transistor Q2 starts to conduct when its base becomes slightly positive. The collector potential of transistor Q2 decreases, reducing the bias to the base of transistor Q1 and tending to cut it off. Again, a regenerative condition is set up and the circuit abruptly returns to its initial stable state with transistor Q2 in saturation and Q1 cut off.

The outputs are taken from the collectors of transistors Q1 and Q2. The waveforms at these points are complementary and essentially square. The time duration of the single-shot is determined by the RC time constant of capacitor C1 and resistor R2.

e. Shift Register

The shift register is a special circuit consisting of several JK flip-flops connected in series. In the Motorola Document Reader, the shift register is used to receive the bits of a full character at one time and then to read them out in sequential or serial form. All portions of the shift register are precleared (before information) at one time and all receive information at one time. They are then triggered by timing pulses to step or shift the information through an output circuit bit by bit.

5. Multiple (Expanded) Inputs

At times it becomes desirable to have more inputs to a circuit than are available on the integrated circuit itself. In that case, expanded or multiple input gates are used. Figure 18 shows an expanded input AND gate and an expanded input OR gate.

When a gate is capable of having an expanded input, the input from the extra input gate is by way

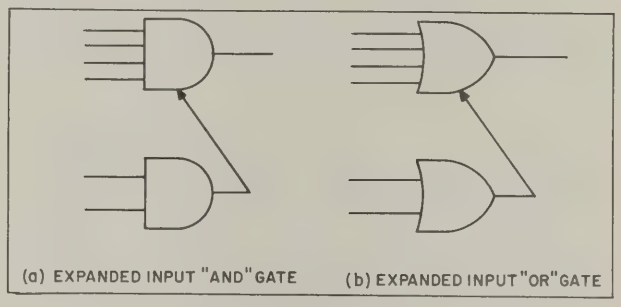


Figure 18. Expanded Input Gates

of a special input terminal, provided during manufacturing for this express purpose. Both of the gates illustrated in Figure 18 are used in the circuits of the Motorola Document Reader.

C. CODES (INPUT/OUTPUT LANGUAGES)

Important to the understanding of the codes is a knowledge of the binary number system. Man learned to count by becoming aware of a direct correlation between his assorted belongings and his fingers. Consequently, he learned to count with his fingers. Because he had ten fingers, the decimal number system was evolved and has been in use ever since.

The method used to write a number using the Arabic numeral system is really a shorthand method. For example:

875 is shorthand for $(8 \times 100) + (7 \times 10) + (5 \times 1)$; in other words eight one hundreds, seven tens and five ones. This same number may also be written as $(8 \times 10^2) + (7 \times 10^1) + (5 \times 10^0)$

Any decimal number can be expressed in this same manner and it can be seen that the ascending powers of 10 represent a practical means of keeping track of the number of ten counts early man made on his fingers when involved with large quantities. The modern Theory of Numbers gives the term "radix" to this base 10 of our decimal system and "coefficients" to the digits 0 through 9. It also shows that number sys-

tems can be devised using any other radix (or base). (If you have any grade school children studying "Modern Math", you are probably already aware of these number systems.)

1. Binary Number System

The binary number system uses the radix 2. It has two coefficients, 0 and 1. If our early ancestors possesed one finger on each hand rather than five, the binary number system would undoubtedly have evolved instead of the decimal number system. At any rate, any quantity which can be expressed decimally can also be expressed in binary form. For example:

The decimal number $17=(1\times10^1)+(7\times10^0)$.
The decimal number 17 written in binary form $=10001_4$ which is shorthand for $(1\times2^4)+(0\times2^3)+(0\times2^2)+(0\times2^1)+(1\times2^0)$.

The binary number system has rules that are much simpler than those of our familiar decimal numbering systems. This simplicity makes the binary numbering system ideal for computers and computer-oriented devices.

Table 4 shows a five-column binary table and the coefficient combinations required for a count from 1 through 16 in decimal form. Notice in the right column (under binary weights) that the 1 and 0 coefficients alternate consistently (binary weight of 1). In the second column from the right, the 1 and 0 alternate in pairs (binary weight of 2). In the third column from the right, the 1 and 0 alternate in sets of four (binary weight of 4) and so on. Therefore, to find the decimal equivalent of any binary series, we can assign a binary weight of 1 to the right column and ascend toward the left assigning 2, 4, 8 and 16 to the succeeding columns. This process may be used and extended for as many columns as exist in the binary combination and is very useful in converting binary counts to decimal equivalents.

To convert the binary combination to a decimal equivalent, find only the 1 coefficients in the binary combination and then follow the column upward to find the corresponding binary weight. After finding the binary weight for each 1 in the binary combination, add these binary weights to find the decimal equivalents. For example:

Binary Combination	1	0	1	0	1	
Binary Weight	16	+ 0	+ 4	+ 0	+ 1	= 21

The decimal equivalent of the binary number 10101 is 21.

Table 4 may be extended to the left to handle larger binary combinations simply by adding the binary weights in ascending order. In other words, the next columns to the left would be 32, 64, 128, 256, etc., and the coefficients would alternate in identical sets 32, 64, 128, 256, etc.

The decimal system requires a memory of ten different coefficients whereas the binary system

BINARY WEIGHTS					DECIMAL WEIGHTS	
16	8	4	2	1	TENS	ONES
0	0	0	0	0	0	0
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	0	1	1	0	3
0	0	1	0	0	0	4
0	0	1	0	1	0	5
0	0	1	1	0	0	6
0	0	1	1	1	0	7
0	1	0	0	0	0	8
0	1	0	0	1	0	9
0	1	0	1	0	1	0
0	1	0	1	1	1	1
0	1	1	0	0	1	2
0	1	1	0	1	1	3
0	1	1	1	0	1	4
0	1	1	1	1	1	5
1	0	0	0	0	1	6

Table 4. Binary to Decimal Equivalents

involves only two. However, as previously pointed out, it requires many more of these binary coefficients in the appropriate combination to represent the same number using decimal coefficients. The human mind has little difficulty in remembering and manipulating ten coefficients so the decimal system works out very well for us. It is much less cumbersome than working with systems having a smaller base. However, in electrical or electronic equipment, it is difficult and uneconomical to design and manufacture circuits having ten discrete, stable and controllable states. It is relatively simple (and economically feasible) to design efficient and reliable bistable circuits that are stable in two states (on or off, energized or de-energized, closed or open, go or no-go, etc.). Therefore, there is a direct correlation between the majority of the digital equipment presently in use and the two-valued binary number system which also provides the basis for symbolic logic. A knowledge of the binary number system provides a valuable aid to the use and understanding of the capabilities of symbolic logic. A knowledge of the binary number system provides a valuable aid to the use and understanding of the capabilities of symbolic logic.

2. Hollerith Code

Dr. Herman Hollerith created and developed a system using the punched card to improve inadequate clerical tabulating methods.

The Hollerith or tab card contains spacing for 80 vertical columns. Each column can store one character of information. Horizontally, the card is divided into 12 data positions, called "rows".

Row numbers "0" through "9" represent strictly numerical data. To represent an alphanumeric character, rows "12", "11", and "0" along with a numeric row ("0" through "9") must be combined according to preset pattern (Refer to Table 5, Code Conversion Chart).

Characters are recorded on a card by punching or marking the specified Hollerith rows. For example, to enter "MDR-1000" on a tab card (Refer to Figure 19):

- determine the Hollerith code for the alphanumeric character "M"; then, in column 1, enter a mark (or punch) in the "11" and "4" data rows.
- determine the Hollerith code for the letter "D"; then, in column 2, enter a mark in the "12" and "4" data rows.
- determine the Hollerith code for the letter "R"' then, in column 3, enter a mark in the "11" and "9" data rows.
- determine the Hollerith code for the – (dash) symbol; then, in column 4, enter a mark in the "11" data row.
- in column 5, enter a mark in the "1" data row
- in column 6, enter a mark in the "0" data row
- in column 7, enter a mark in the "0" data row
- in column 8, enter a mark in the "0" data row.

The card now contains the information (MDR-1000) in a Hollerith code. The MDR would read this information and convert the data to its particular output language.

There are several important points to be noted. First, a value consisting of two or more numbers or a word must be punched or marked in CONSECUTIVE columns. Second, for a numeric only reader, if more than one data row is punched or marked in a column, the machine will not be able to decode that column correctly. Finally, to represent letters and most symbols, two or more data rows must be punched or marked in a column.

3. USASCII Code

The USA Standard Code for Information Interchange is a common machine language used for the general interchange of information among processing systems , communication systems and associated equipment. It is a 7-bit plus parity code that provides the necessary alphanumeric graphics, special codes, and communication and device controls required for interchanging information.

Table 5, Code Conversion Chart, shows the characters to be coded and their relationship to the Hollerith code and other codes.

4. EBCDIC Code

The Extended Binary Coded Decimal Interchange Code is an 8-bit code with no parity. This is an IBM code used internally in the System 360® computers. When peripheral gear utilizes this code, there is no need for interface translation. The code consists of 159 characters; alphanumerics, special graphics, and machine control codes.

Table 5, Code Conversion Chart, shows the characters to be decoded and their relationships to the EBCDIC code and other codes.

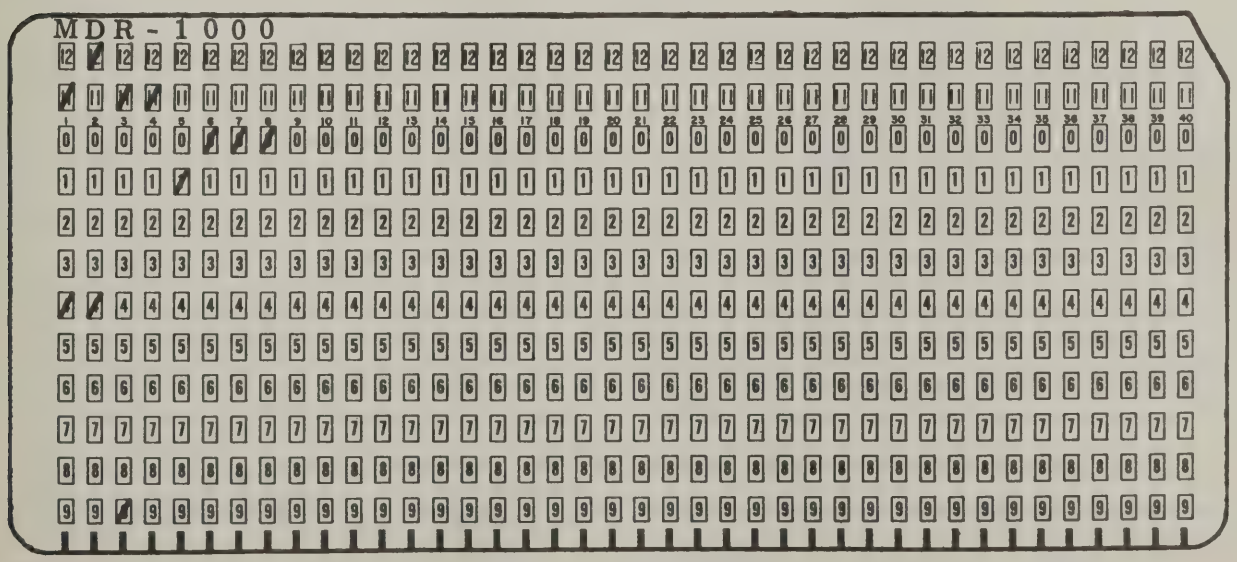


Figure 19. "MDR-1000" Entered on Tab Card in Hollerith Code

PARITY LAMP ON UNEVEN ONES (TEST SET)

INPUT HOLLERITH PUNCH POSITIONS	OUTPUT USASCII 1234567C	OUTPUT PTTC/BCD BA8421C	OUTPUT EBCDIC◊ 76543210
NO PUNCHES	SP 0000010C*	SP 000000C	SP 00000010
1	1 1000110C	1 000001C	1 10001111
2	2 0100110C	2 000010C	2 01001111
3	3 1100110C	3 000011C	3 11001111
4	4 0010110C	4 000100C	4 00101111
5	5 1010110C	5 000101C	5 10101111
6	6 0110110C	6 000110C	6 01101111
7	7 1110110C	7 000111C	7 11101111
8	8 0001110C	8 001000C	8 00011111
9	9 1001110C	9 001001C	9 10011111
0	Ø 0000110C	Ø 001010C	Ø 00001111
0-1	/ 1111010C	/ 010001C	/ 10000110
0-2	S 1100101C	S 010010C	S 01000111
0-3	T 0010101C	T 010011C	T 11000111
0-4	U 1010101C	U 010100C	U 00100111
0-5	V 0110101C	V 010101C	V 10100111
0-6	W 1110101C	W 010110C	W 01100111
0-7	X 0001101C	X 010111C	X 11100111
0-8	Y 1001101C	Y 011000C	Y 00010111
0-9	Z 0101101C	Z 011001C	Z 10010111
0-8-1	: 0011111C	‣ 011011C	10010110
0-8-2	\ 0011101C	± 011010C	\ 00000111
0-8-3	, 0011010C	‣ 011011C	11010110
0-8-4	% 1010010C		% 00110110
0-8-5	— 1111101C		— 10110110
0-8-6	> 0111110C	— 100000C	> 01110110
0-8-7	? 1111110C	± 001011C	? 11110110
0-9-2			01000100
0-9-3			11000100
0-9-4		BY 011100C	BYP 00100100
0-9-5	LF 0101000C	LF 011101C	LF 10100100
0-9-6		EOB 011110C	ETB 01100100
0-9-7	ESC 1101100C	PRE 011111C	ESC 11100100
0-9-8-3			11010100
0-9-8-4			00110100
0-9-8-5			ENQ 10110100
0-9-8-6			ACK 01110100
0-9-8-7	BEL 1110000C		BEL 11110100
8-1			` 10011110
8-2	: 0101110C		: 01011110
8-3	# 1100010C	# 001011C	# 11011110
8-4	@ 0000001C	@ 010000C	@ 00111110
8-5	' 1110010C		' 10111110
8-6	= 1011110C		= 01111110
8-7	" 0100010C		" 11111110
9-1			10001100
9-2			SYN 01001100
9-3			11001100
9-4		PN 001100C	PN 00101100
9-5		RS 001101C	RS 10101100
9-6		UC 001110C	UC 01101100
9-7	EOT 0010000C	EOT 001111C	EOT 11101100
9-8-1			10011100
9-8-2			01011100
9-8-3			11011100
9-8-4	DC4 0010100C		DC4 00111100
9-8-5			NAK 10111100
9-8-6			01111100
9-8-7			SUB 11111100
11	- 1011010C	- 100000C	- 00000110
11-0	SHIFT** C	MZ 101010C**	} 00001011**
11-1	J 0101001C	J 100001C	J 10001011
11-2	K 1101001C	K 100010C	K 01001011
11-3	L 0011001C	L 100011C	L 11001011
11-4	M 1011001C	M 100100C	M 00101011
11-5	N 0111001C	N 100101C	N 10101011
11-6	O 1111001C	O 100110C	O 01101011
11-7	P 0000101C	P 100111C	P 11101011
11-8	Q 1000101C	Q 101000C	Q 00011011
11-9	R 0100101C	R 101001C	R 10011011
11-0-2			ş 01000101
11-0-3			¢ 11000101
11-0-4			u 00100101
11-0-5			v 10100101
11-0-6			w 01100101
11-0-7			x 11100101
11-0-8			y 00010101
11-0-9			z 10010101

INPUT HOLLERITH PUNCH POSITIONS	OUTPUT USASCII 1234567C	OUTPUT PTTC/BCD BA8421C	OUTPUT EBCDIC◊ 76543210
11-8-1	` 0000011C		10011010
11-8-2	] 1011101C	! 101011C	] 01011010
11-8-3	$ 0010010C	$ 101011C	$ 11011010
11-8-4	* 0101010C		* 00111010
11-8-5	) 1001010C		) 10111010
11-8-6	; 1101110C		; 01111010
11-8-7	^ 0111101C	¢ 010000C	^ 11111010
11-9-1	DC1 1000100C		DC1 10001000
11-9-2	DC2 0100100C		DC2 01001000
11-9-3	DC3 1100100C		DC3 11001000
11-9-4		RES 101100C	RES 00101000
11-9-5		NL 101101C	NL 10101000
11-9-6		BS 101110C	BS 01101000
11-9-7		IL 101111C	IL 11101000
11-9-8			CAN 00011000
11-9-8-1			EM 10011000
11-9-8-2			CC 01011000
11-9-8-3			11011000
11-9-8-4	FS 0011100C		FS 00111000
11-9-8-5	GS 1011100C		GS 10111000
11-9-8-6	RS 0111100C		RS 01111000
11-9-8-7	US 1111100C		US 11111000
12	& 0110010C	& 110000C	& 00001010
12-0	{ 1101111C	PZ 111010C	{ 00000011
12-1	A 1000001C	A 110001C	A 10000011
12-2	B 0100001C	B 110010C	B 01000011
12-3	C 1100001C	C 110011C	C 11000011
12-4	D 0010001C	D 110100C	D 00100011
12-5	E 1010001C	E 110101C	E 10100011
12-6	F 0110001C	F 110110C	F 01100011
12-7	G 1110001C	G 110111C	G 11100011
12-8	H 0001001C	H 111000C	H 00010011
12-9	I 1001001C	I 111001C	I 10010011
12-11	EJECT***	EJECT***	EJECT***
12-0-1			a 10000001
12-0-2			b 01000001
12-0-3			c 11000001
12-0-4			d 00100001
12-0-5			e 10100001
12-0-6			f 01100001
12-0-7			g 11100001
12-0-8			h 00010001
12-0-9			i 10010001
12-8-1	~ 0111111C	· 111011C	10010010
12-8-2	[1101101C	? 010001C	[01010010
12-8-3	· 0111010C	· 111011C	· 11010010
12-8-4	< 0011110C		< 00110010
12-8-5	(0001010C		(10110010
12-8-6	+ 1101010C	+ 110000C	+ 01110010
12-8-7	! 1000010C		! 11110010
12-9-1			SOH 10000000
12-9-2			STX 01000000
12-9-3			ETX 11000000
12-9-4		PF 111100C	PF 00100000
12-9-5	HT 1001000C	HT 111101C	HT 10100000
12-9-6		LOC 111110C	01100000
12-9-7	DEL 1111111C	DEL 111111C	DEL 11100000
12-11-1			j 10001001
12-11-2			k 01001001
12-11-3			l 11001001
12-11-4			m 00101001
12-11-5			n 10101001
12-11-6			o 01101001
12-11-7			p 11101001
12-11-8			q 00011001
12-11-9			r 10011001
12-9-8-1			10010000
12-9-8-2			SMM 00001010
12-9-8-3	VT 1101000C		VT 11010000
12-9-8-4	FF 0011000C		FF 00110000
12-9-8-5	CR 1011000C		CR 10110000
12-9-8-6			SO 01110000
12-9-8-7			SI 11110000
12-11-0-1			10001101
12-11-0-2			01001101
12-11-0-3			11001101
12-11-0-4			00101101
12-11-0-5			10101101
12-11-0-6			01101101
12-11-0-7			11101101
12-11-0-8			00011101
12-11-0-9			10011101

* "C" is odd or even parity bit.

** "SHIFT" code optional. When used, the 11-0 Hollerith positions are marked along with the desired output code in Hollerith positions 1 thru 7 (USASCII), 1 thru 6 (PTTC/BCD) or 1 thru 8 (EBCDIC). Hollerith input codes containing marks in the 11-0 rows become illegal when this option is provided.

*** "EJECT" code optional. If used, all codes containing the Hollerith punch positions 12-11 will be recognized as the MDR machine language "EJECT" and no output will be generated.

◊ Codes not illustrating a graphic or control symbol are unassigned within the coding structure. They are, however, valid and are generated by the MDR when the corresponding card code appears on the document.

Table 5. Code Conversion Chart

LEGEND FOR TABLE 5.

ACK	Acknowledge	RES	Restore
BEL	Bell	RS (USASCII)	Record Separator
BS	Backspace	RS (PTTC/BCD)	Reader Stop
BY	Bypass	SI	Shift In
BYP	Bypass	SMM	Undefined
CAN	Cancel	SO	Shift Out
CC	Undefined	SOH	Start of Heading
CR	Carriage Return	Sp	Space
DC1	Device Control 1	STX	Start of Text
DC2	Device Control 2	SUB	Substitute
DC3	Device Control 3	SYN	Synchronous Idle
DC4	Device Control 4	UC	Upper Case
DEL	Delete (Rubout)	US	Unit Separator
EM	Undefined	VT	Vertical Tabulation
ENQ	Enquiry	IL	Idle
EOB	End of Block	LOC	Lower Case
EOT	End of Transmission	LF	Line Feed
ESC	Escape	MZ	Minus Zero
ETB	End of Transmission Block	NAK	Negative Acknowledge
ETX	End of Text	NL	New Line
FF	Form Feed	PF	Punch Off
FS	File Separator	PN	Punch On
GS	Group Separator	PRE	Prefix
HT	Horizontal Tabulation	PZ	Plus Zero

5. PTTC/BCD - PTTC/EBCD Codes

These are IBM Paper Tape Transmission Codes/ Binary Coded Decimal and Extended Binary Coded Decimal. While the bit structure of the two languages are identical, the graphics vary due to keyboard differences in the business machines in which the particular code is used. The Data Card Codes (Hollerith) used to generate the particular PTTC language will also have variations from one machine to another. Typically, these are codes used in Selectric® typewriters in communications systems. The code has a 6-bit plus parity structure. It includes 72 characters of alphanumeric, special graphics, and machine control codes.

Table 5, Code Conversion Chart, shows the characters to be decoded and their relationship to the PTTC/BCD code and other codes.

D. DOCUMENTS

The design characteristics of a readable document are so flexible that documents exist on many types of forms and in various formats. It will be the responsibility of the technician to recognize when a document does not meet the required specifications and to relate this information to the customer in terms that he can understand.

A useful document-troubleshooting aid is the IBM Registration Gauge #450770. This gauge can be used to check the registration of all data columns, format marks and data rows on a standard keypunched tab card.

The reading area for any type of document is confined to a 3-1/4 inch strip along the edge of the document. Within the reading area, 12 fixed, data row positions

CHARACTERISTIC	80-COLUMN CARD*	PAGE
Length	7.375" ± 0.005"	4.875" minimum up to any practical length
Width	3.250" + 0.007" -0.003"	3.250" minimum up to 8.50" ± 0.10"
Thickness	0.007" ± 0.0004"	0.0055" + 0.002" -0.001"
Weight (500 sheets 25" x 38")	N/A	50 lb. book (20 lb. bond)
Composition	100 percent chemical wood fiber	100 percent chemical wood fiber or any commercially available uncoated paper suitable for offset printing.

*Card specifications apply for all applications involving keypunching and/or hopper fed MDR machines. Width and thickness tolerances can be reduced for manually marked and manually fed cards: width ±0.010", thickness ±0.001". Length can also be shortened to 4.875".

Table 6. Specifications for Documents

(corresponding to the phototransistor sensors within the MDR sensing head) comprise each data column. Each data column has a corresponding format mark at its base.

The MDR sensing head contains a light source and 13 phototransistors (one for each of the 12 data rows and one for reading the format marks). When light is reflected into the lens of a phototransistor, a quiescent or no signal state exists. When reflected light is diffused in a particular data block – either by pencil mark, punched hole, or preprinted mark – the corresponding phototransistor yields a signal output.

The no signal or quiescent state must be a characteristic of the basic document before data can be entered. Therefore, card or paper stock should be white, natural, yellow or buff colored. Other colors may be used, but should have been previously tested for reading sensitivity.

Table 6 lists all the specifications for the various documents available.

Four basic formats are generally used: 80-column (keypunch); 40-column, 2-color; 40-column, 1-color and a combination 40- and 80-column format. (Refer to Figure 7 for an illustration of the various forms and formats available.)

For 1-color applications, the entire information must be printed in non-reflective ink. For 2-color applications, the punch or mark positions, headings, notes, and other information in the readable area (excluding format marks) must be printed in reflective red ink. The format marks must be printed in non-reflective, black ink.

V. PRELIMINARY SYSTEM ANALYSIS

A. OVERALL OPERATION OF READER

1. Physical Layout of MDR

The Motorola Document Reader consists of three major assemblies: Power Supply, Card Transport and Card Cage (electronics.) Figure 20 shows the physical layout of the MDR.

The power supply provides the following output voltages: 117 Vac, +15 Vdc, +12 Vdc, -12 Vdc, +5 Vdc, +lamp supply, -lamp supply, power common and relay common. Three independent, regulated power supplies with voltage overload protection generate the output voltages.

The card transport is the mechanical heart of the unit. It stores, feeds, positions, controls, and retrieves cards when operated in the automatic mode. (In the manual mode, the card transport simply positions and controls the document as it passes through the unit.)

The card cage contains the electronic circuitry required to read, translate, and transmit the data from the input document to the interface device. Amplifiers and storage registers obtain the data. Decoders/encoders translate the data (Hollerith) to the required output language. Timing, control, and interface logic then transmit the converted data to the receiving terminal.

2. Basic Block Diagram (Refer to Figure 21)

When the POWER switch is pressed, the input ac power is applied to an input transformer. The secondary of this transformer then applies power to three independent, regulated power supplies: lamp power supply, integrated circuit power supply, and component power supply. All units that operate in the attended mode will also have ac power applied to the motor in the card transport.

The lamp power supply generates two positive lamp voltages and a negative lamp voltage. This supply monitors the voltage drop across the lamps in the sensing head. If the lamps are all lighted, the lamp power supply provides an output voltage to light the READY indicator on the operator's panel. The lamp power supply also generates a -12 Vdc voltage for the interface converter which

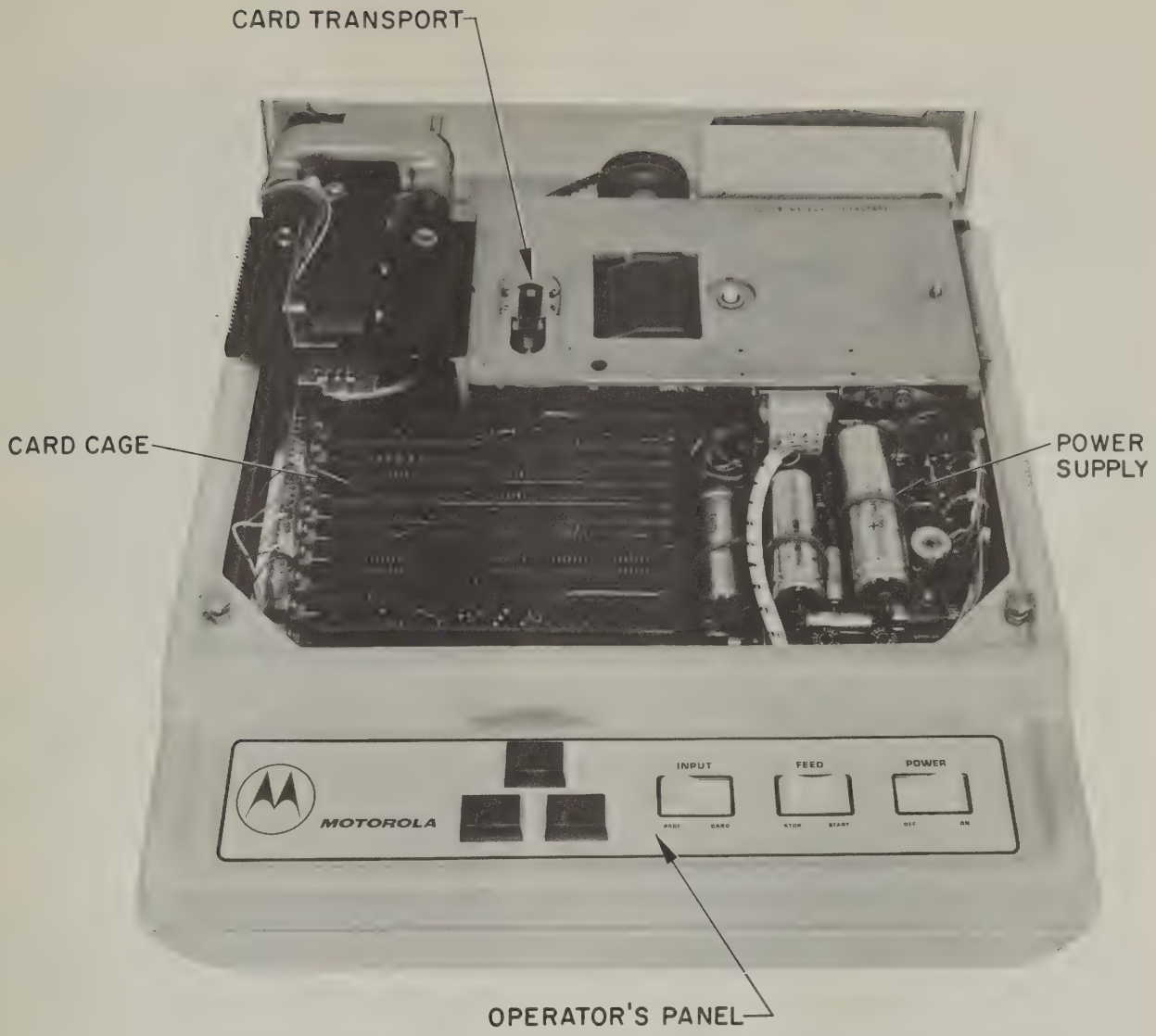


Figure 20. Physical Layout of MDR

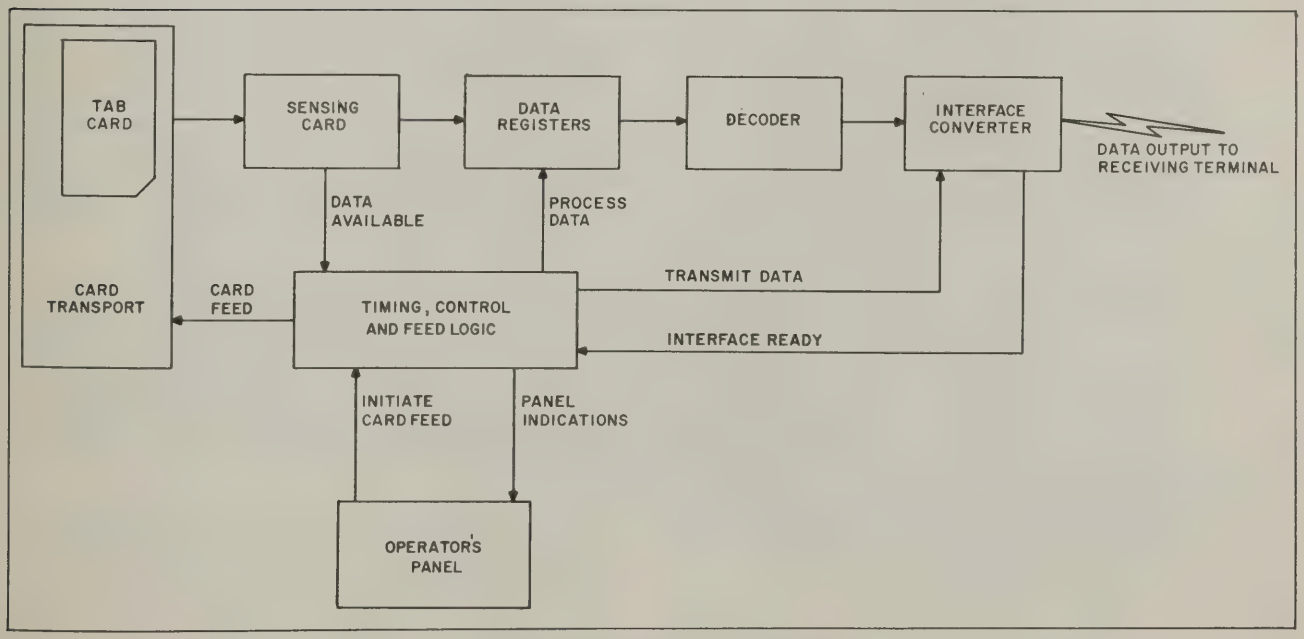


Figure 21. Basic Block Diagram

may or may not be required for the particular model in use.

The integrated circuit power supply generates a +5 Vdc voltage. This regulated voltage is protected by a SCR crow bar circuit. A positive 1.2 volt deviation in the output automatically triggers the SCR circuit. With the SCR circuit energized, the input stage for the power supply is shorted. This causes the fuse in the secondary of the transformer to blow, preventing damage to the integrated circuits used within the unit.

The component power supply generates the +12 Vdc voltages. The +12 Vdc voltage is used for the discrete components, while +15 Vdc is used for the card feed solenoid in the card transport. Neither voltage is adjustable. The +12 Vdc supply is protected by a voltage controlled SCR circuit, similar to the circuit used in the integrated circuit power supply.

With the READY indicator on, the operator may now establish communications with the receiving device. When a valid connection has been established, the SEND indicator will light.

At this time, the input document passes through the sensing head. Lamps in the sensing head provide a light source for the phototransistors to detect the presence of data.

When light is reflected into the phototransistor, a quiescent or no signal state exists. When the reflected light is diffused – either by pencil mark, punched hole, preprinted mark, pen mark, or format mark – the corresponding phototransistor yields a signal output.

The outputs of the phototransistors are amplified and stored in data registers.

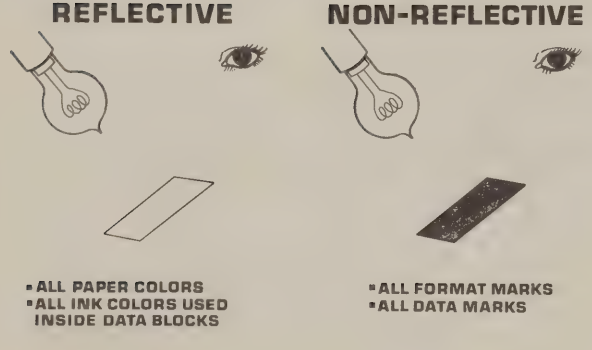


Figure 22. Phototransistor Data Sensing

When the sensing head detects the format mark on the document, it notifies the timing and control logic. This event initiates the processing of the data and presets the interface converter in a state ready to transmit the converted data.

The data is transferred out of the data registers into the deconding circuitry. Here the language of the incoming data is manipulated to conform to the language required by the receiving device. The output of the decoder is then transferred through the interface converter to the receiving terminal. This output is controlled by the internal timing of the MDR and may be either in serial or in parallel form, depending upon the requirements of the receiving device.

3. Transport Mechanism (Refer to Figure 23)

All mechanical functions relating to the feeding, positioning, speed, ejection, and retrieval of a document are performed by the transport mechanism.

The basic transport mechanism consists of a motor which drives the speed control pulleys, main drive shaft and drive rollers. Automatic feed units incorporate into the basic transport mechanism (1) a feed roll assembly along with its associated drive shaft, pulleys and belts, (2) an eject drive roller along with its associated pulleys and belt, and (3) a clutched shaft assembly.

Only one control signal is required by the transport mechanism and that signal is to the feed solenoid for an automatic card feed. Two switches are used in the transport mechanism: one is the hopper empty switch, which informs the Document Reader as to the status of the hopper, and the other is the filler plate switch which prevents the feed roller from operating if a hopper is not installed in the unit.

B. OPERATION WITH INTERFACE EQUIPMENT

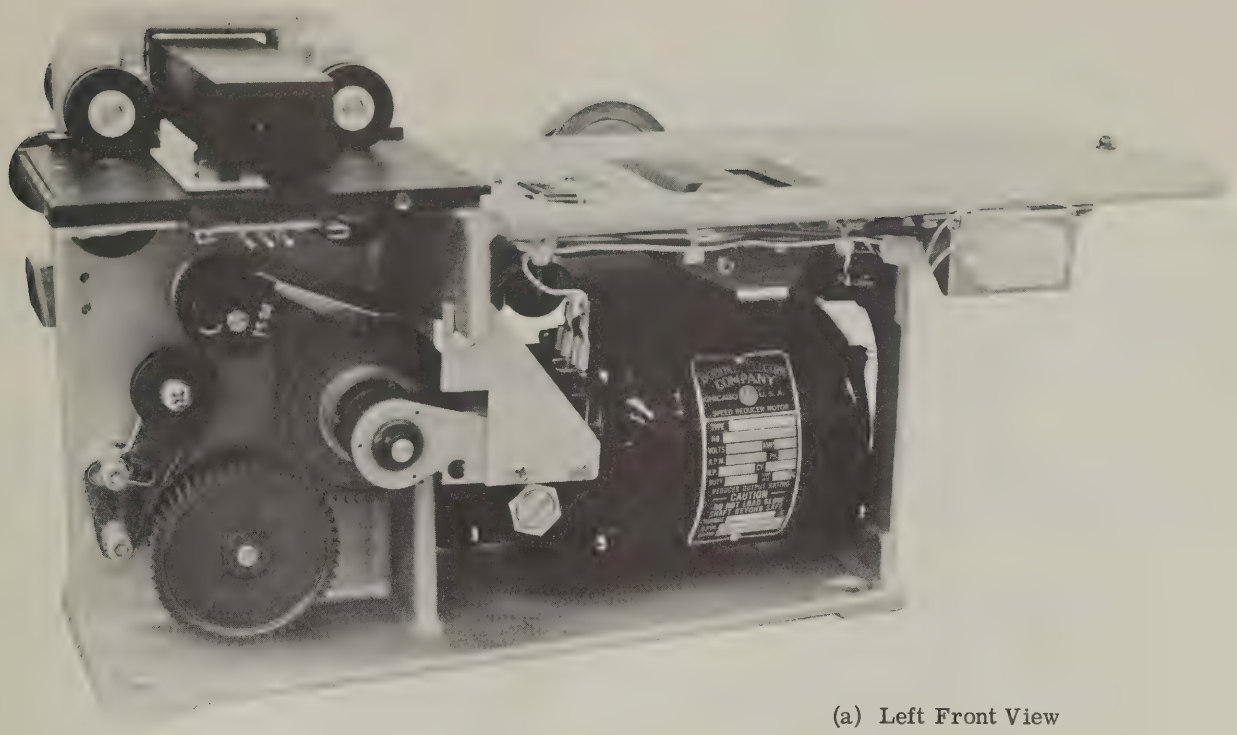
The Motorola Document Reader operates with many types of interface devices: business machines and modems being the most common. Each interface device is designed to accept data in a specific format and at a definite rate; therefore, modifications are necessary to the basic Document Reader. These modifications are reflected in the model number of the unit.

Each character transmitted to an interface device must conform to a specific bit pattern in order for the interface device to separate the incoming characters.

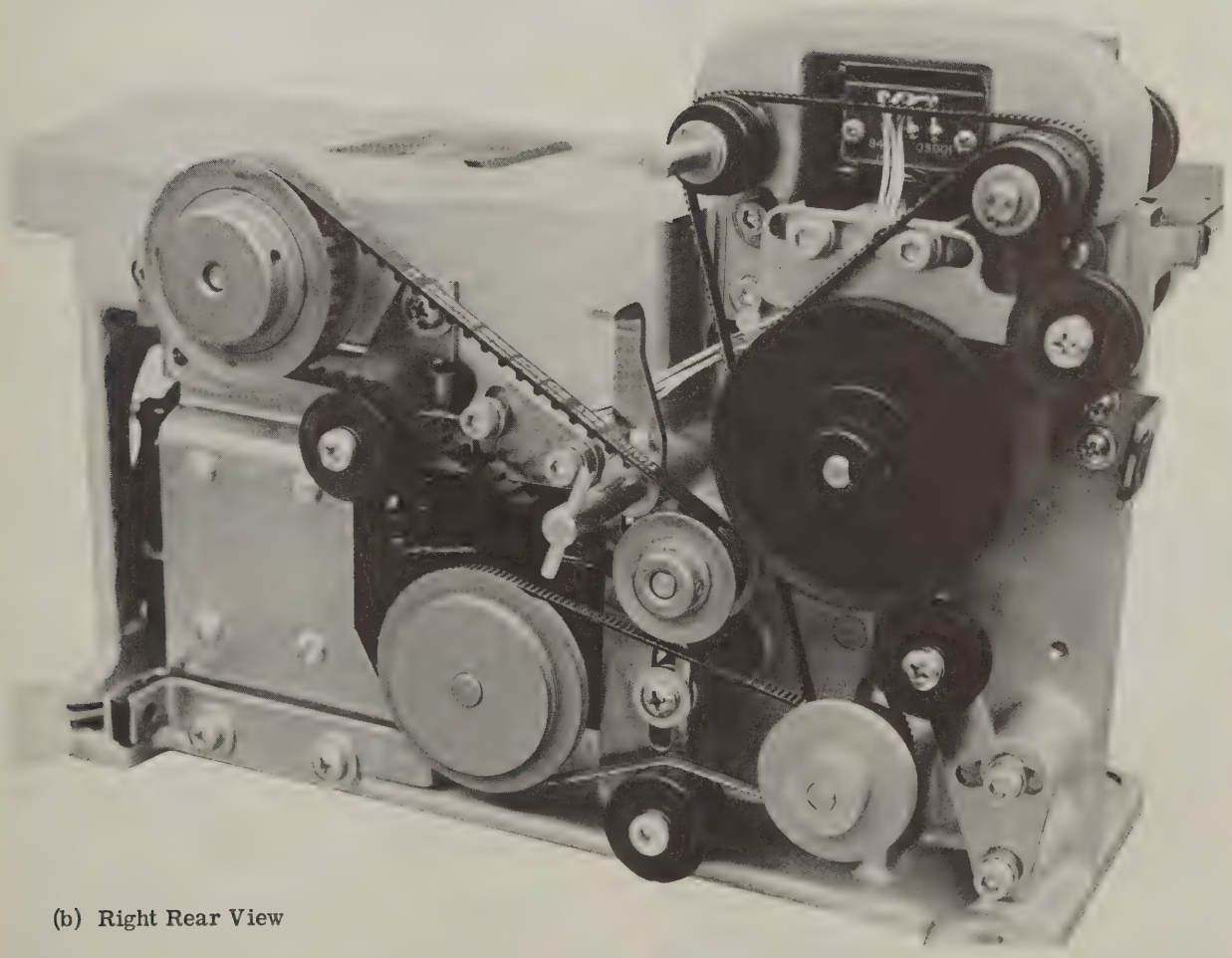
All high speed receiving devices require a 10-bit input message structure as shown in Figure 24.

In Figure 24, each bit in the message is allotted a fixed time. The "ON" bit (SPACE) indicates the beginning of a character. The 8-bits of data are followed by an "OFF" bit (MARK).

When transmitting data in USASCII code, bits 1 thru 7 contain the coded character and bit 8 is a parity



(a) Left Front View



(b) Right Rear View

Figure 23. Transport Mechanism

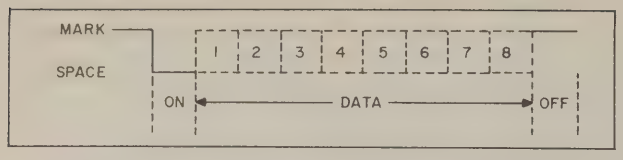


Figure 24. High Speed Message Structure

bit. When transmitting data in a PTTC/BCD code, bits 1 thru 6 contain the coded character, bit 7 is a parity bit, and bit 8 is forced to a MARK condition. This essentially provides two "OFF" (MARK) bits to end the message. When transmitting data in an EBCDIC code, bits 1 thru 8 contain the coded character.

Low speed receiving devices require either a 9-, 10-, or 11-bit message structure, depending upon the language used. Figure 25 shows the various message structures required.

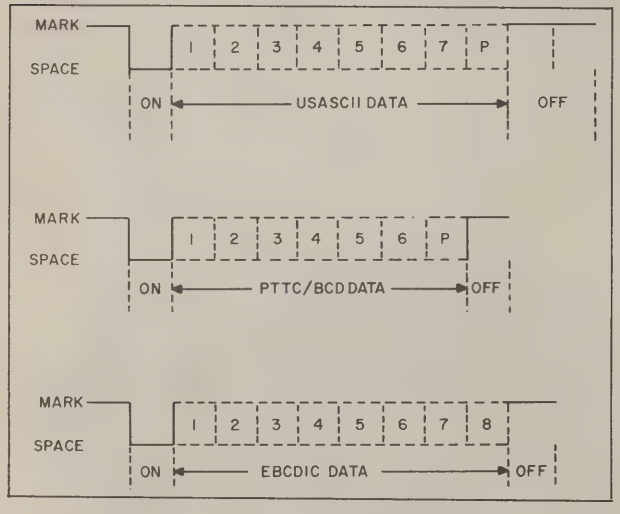


Figure 25. Low Speed Message Structure

In Figure 25, the USASCII data requires 11 bits; this varies from the high speed message in that two "OFF" (MARK) bits are necessary when transmitting at low speed. The PTTC/BCD message structure requires one less "OFF" bit when transmitting at low speed; this reduces its message length to 9-bits. The EBCDIC message structure is the same regardless of the transmission speed.

1. Teletypewriter Sets (Refer to Figure 27b)

   The Motorola Document Reader interfaces to many types of teletypewriter sets. Teletypewriter sets can perform page printing, keyboard entry, paper tape punching, and paper tape reading. Some units provide all of these features; others provide only a portion of the features.

   The MDR supplies a normally-closed dry contact output which is connected into a current loop. Teletypewriter sets use a 20 or 60 mA input circuit. The MDR is inserted into this circuit as shown in Figure 26.

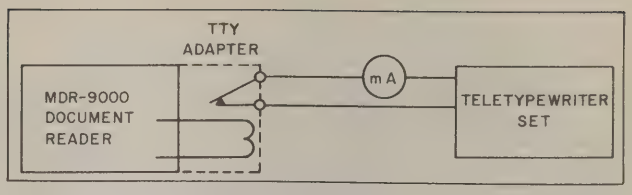


Figure 26. Typical Teletypewriter Set Connection

When data is transmitted, the contact is opened and closed at a predetermined rate. Teletypewriter sets are low speed devices that accept data at the rate of 10 characters/second (110 bits/second) in a USASCII code.

The "ON" bit (a SPACE) indicates the beginning of a character. This is accomplished by breaking the input current loop which informs the teletypewriter set that a message is coming. The specific data then follows. In this case, the data is coded in USASCII (7-bits plus a parity "P" bit). The data portion of the message is then followed by two "OFF" bit times. The return to a MARK (closed current loop) condition for two bit time periods informs the teletypewriter set that the character is finished. The next character can then be sent by sending a SPACE (breaking the current loop) or "ON" bit. This process will continue until all data has been transmitted.

2. Modems

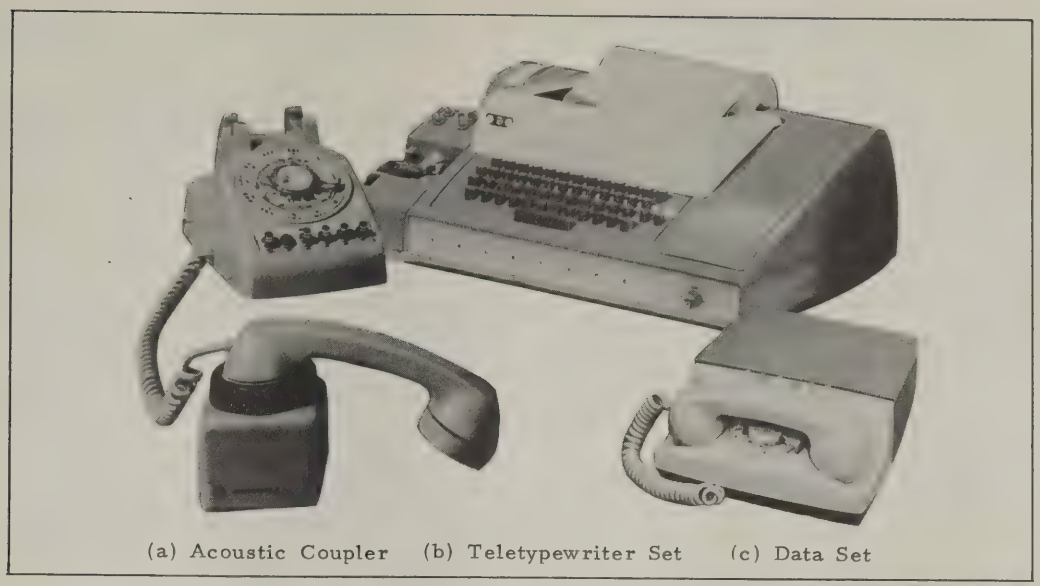
   Modems are devices that accept digital information, convert it to a tone and then transmit the information over standard telephone communication lines to a receiving terminal. The receiving terminal then converts the tone back to digital information. Modems can be classified into two groups: data sets (refer to Figure 27c) and acoustic couplers (refer to Figure 27a).

   Acoustic couplers are low speed, attended units. Data sets vary in transmitting speed, are normally fixed to a location, and provide many automatic features that are not possible to obtain with an acoustic coupler.

   Both devices must meet the EIA Standard – Voltage Interface RS-232B. This standard sets forth the method for transmitting data, the protective circuitry required, and type of control signals used.

   When transmitting data using an acoustic coupler, the operator places a call over the dial-up telephone network to the receiving terminal. The telephone handsets at both locations are then inserted into the acoustic couplers. All documents are then fed through the MDR. Some of the more common acoustic couplers available are manufactured by Motorola (MDR-3000 series), Omnitec, General Electric, Anderson-Jacobson, and DATA Communications Systems.

   Data sets, on the other hand, require the presence of special control signals before any data may be transmitted. These control signals are automatically generated by the union of the MDR with its transmitting data set and the remotely



(a) Acoustic Coupler (b) Teletypewriter Set (c) Data Set

Figure 27. Typical Interface Devices

located receiving data set. Figure 28 shows the signals necessary for transmitting data.

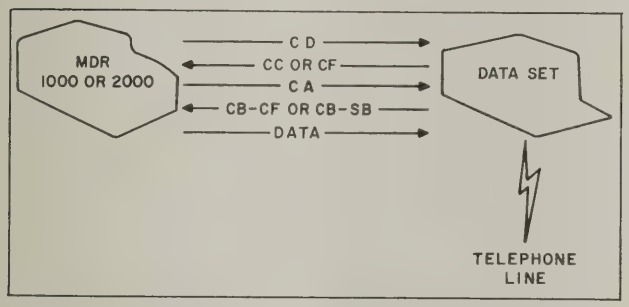


Figure 28. Required Control Signals for Transferring Data

The MDR provides a CD signal (Data Terminal Ready) to the data set. The data set returns a CC signal (Data Set Ready) or a CF signal (Data Carrier Detector). The MDR then requests to send data (CA-Request to Send). The presence of CB and CF signals (Clear to Send - Data Carrier Detector) or CB and SB signals (Clear to Send - Reverse Channel) to the MDR initiates the authorization to transmit.

Many different models of data sets exist; therefore there are variations in the required control signals relative to the data sets. To compensate for this, the MDR uses screw-on terminal straps on several circuit boards for routing input control signals and for enabling the internal data set security circuits.

For all serial output machines, output connector J15 is wired as shown in Figure 29.

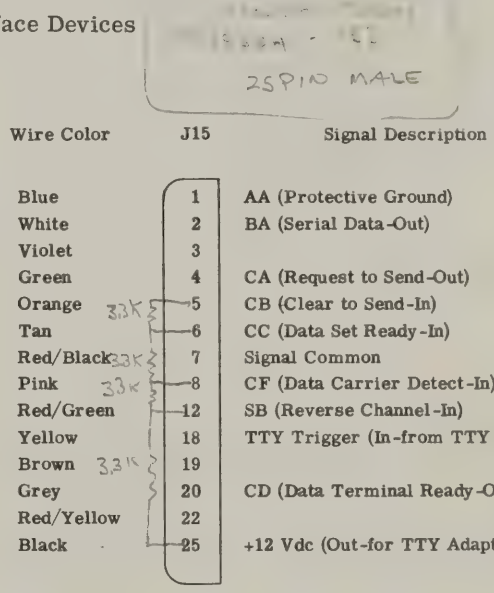

25 PIN MALE
Wire Color
J15
Signal Description
Blue 1 AA (Protective Ground)
White 2 BA (Serial Data-Out)
Violet 3
Green 4 CA (Request to Send-Out)
Orange 33K 5 CB (Clear to Send-In)
Tan 6 CC (Data Set Ready-In)
Red/Black 33K 7 Signal Common
Pink 33K 8 CF (Data Carrier Detect-In)
Red/Green 12 SB (Reverse Channel-In)
Yellow 18 TTY Trigger (In-from TTY Adapter)
Brown 33K 19
Grey 20 CD (Data Terminal Ready-Out)
Red/Yellow 22
Black 25 +12 Vdc (Out-for TTY Adapter)

Figure 29. Output Connector J15, Serial Output Machines

3. Parallel Interfaces

The MDR can directly interface to many types of business machines. Data is transferred by character rather than by bit. The output language of the MDR can be in USASCII, PTTC/BCD, EBCDIC, or Hollerith; therefore, the number of bits per character will vary. Figure 30 shows the wiring of output connector J15 for a parallel output machine.

The MDR supplies the following output signals:

- Data lines and strobe are active (or logical "1") when at +5 Vdc and are inactive (or logical "0") when at ground.
- LE/TE signal is at +5 Vdc when document is under read head and at ground when no document is under read head.
- Hopper Empty signal at ground indicates that there are cards in hopper. A +12 Vdc signal indicates hopper is empty.

Wire Color	J15	Signal Description
	1	Not Used
Violet	2	Data 1, or Hollerith "2" (Out)
Grey	3	Data 2, or Hollerith "3" (Out)
White	4	Data 3, or Hollerith "4" (Out)
Black	5	Data 4, or Hollerith "5" (Out)
Yellow/Green	6	Strobe (Out)
Yellow/Black	7	Data 5, or Hollerith "6" (Out)
Yellow/Brown	8	Data 6, or Hollerith "7" (Out)
Yellow/Red	9	Data 7, or Hollerith "8" (Out)
Yellow/Orange	10	Data 8 (Parity), or Hollerith "9" (Out)
Green	11	Signal Ground
Brown	12	Hollerith "12" (Out)
Orange	13	Hollerith "11" (Out)
Yellow	14	Hollerith "0" (Out)
Blue	15	Hollerith "1" (Out)
White/Black	16	Card Feed Enable (In)
Yellow/Violet	17	LE/TE (Out)
White/Red	18	Hopper Empty Switch (Out)
White/Brown	19	Strobe Reset (In)
Yellow/Grey	20	Data Reset (In)
White/Orange	21	Motor Enable (In)
Yellow/Blue	22	End of Card Pulse (Out)
	23	Not Used
	24	Not Used
Red	25	+12 Vdc (Out)

Figure 30. Output Connector J15, Parallel Output Machines

- End of Card signal, normally at ground, rises to +5 Vdc for 20 to 50 milliseconds as card leaves read head.

Inputs to the MDR from the interface device must meet the following conditions:

- Card Feed Enable (when remote card feed control is required) may be controlled by applying and removing a ground potential signal to pin 16 of J15. If ground potential is not reapplied to pin 16, all cards will feed. If cards are to be fed using the FEED switch, pin 16 must be open.
- Motor Enable control (when remote control of motor is required) may be performed by applying (stop) and removing (start) a ground potential signal to pin 21 of J15.
- Strobe Reset and Data Reset signals can be applied to the MDR by applying a ground potential to pins 19 and/or 20 of J15 for a minimum of 500 nanoseconds. Normally, strobe and data lines are reset when the MDR senses a new character.

All inputs from interface equipment must meet the following voltage requirements:

- Low or ground potential - 0 to 0.5 Vdc
- High - no connection or +5.0 ±0.5 Vdc; +12 Vdc maximum for Data Reset and Strobe Reset only.

VI. COMPREHENSIVE FUNCTIONAL ANALYSIS

The general operation of the Motorola Document Reader has been covered in the previous section A very basic block diagram was used for the previous explanation. In this section, a more detailed analysis of all portions of the MDR will be covered. Both modes of operation, serial and parallel, will be discussed along with the operation for decoding and encoding all output languages.

A. BLOCK DIAGRAMS (Refer to Figures 47 and 48)

Since there are two modes of operation, two block diagrams are used to explain the operations. Since there is much similarity, a full discussion of the serial mode will permit the discussion of the parallel mode to be limited to the differences existing between the two modes of operation.

1. Serial Operation (Refer to Figure 47)

Each data row on a document has a corresponding phototransistor in the sensing head. There is also a phototransistor for the Format Mark, the Leading Edge of a document and the Trailing Edge of a document. These phototransistors are illuminated by the Sensor Lamps and produce signals when data is present on the document. Each phototransistor supplies an input to a Sensor Amplifier. The L.E., T.E., and Format Clock sense amplifiers (Location No. 2) supply signals to the L.E., T.E., and Clock Logic circuitry on the TIMING and CONTROL LOGIC board (Location No. 7). Trailing Edge signals are also supplied to the FEED LOGIC board (Location No. 9) and to the ALARM/BEL board (Location No. 10). All of these input signals are used for control functions.

The data row sense amplifiers (12), which receive parallel information from the data row phototransistors, supply parallel information to the Data Registers (Location No. 3). The data registers enable selection of either normal Hollerith information from a document or inverted information from a document by means of a CARD - PAGE switch located on the operator's panel. Besides the data inputs, the data registers receive a DC REGISTER (Clear) which resets or clears the registers of information and a GATED CLOCK (Window) which sets data into the registers. Each data register has two outputs. Therefore, for each input data signal, two output signals are produced to be used for information. The 12 data registers have a total of 24 data outputs.

Parallel information from the data registers is applied to the DECODER boards. The decoder boards are located in Locations No. 4, 5 and 6. Only one type of decoder uses all three locations. If a board is not needed in a particular location, that slot is left open. There are five types of codes (output languages) available, converted

from a Hollerith input. These are USASCII-85 Character (3boards), USASCII-15 Character (1 board), PTTC/BCD (1 board), EBCDIC (2 boards) and 12 BIT HOLLERITH (1 board). In addition, three of the decoders (USASCII-85 Character, PTTC/BCD and EBCDIC) contain a special function (SHIFT) which enables that particular code to be marked on the document and encoded into the output.

Whichever output language is desired in the output of the Motorola Document Reader determines which board or boards will be used. Each of the decoders receive, in addition to the inputs from the data registers, control function signals such as GATED CLOCK (Window) and PRE and POST CARD PROGRAM CODES. These signals are used to initiate and control the decoding and encoding of the various languages. Other signals, such as (a), (b), (c), etc., are interconnected between boards for the purpose of facilitating decoding. These signals are generated on the decoder boards.

All outputs from the decoder board, after proper encoding, are applied to the TIMING and CONTROL LOGIC board. The information, in parallel form, is applied to input gates for the SHIFT REGISTER. The TIMING and CONTROL LOGIC board (Location No. 7) contains the L.E., T.E. and Format Clock logic, the SHIFT REGISTER, a ÷ 10 COUNTER, a PARITY GENERATION circuit plus various gates used to produce signals such as GATED CLOCK (Window), GATED CLOCK (Logic) and DC REGISTER (Clear).

The TIMING and CONTROL LOGIC board processes the L.E., T.E. and FORMAT CLOCK signals into control signals, generates the PRE and POST CARD PROGRAM CODES, produces serial data from parallel input data, activates the circuitry to produce a card feed and supplies the input to the data output circuits. The control signals are applied to boards in Locations No. 3, 4, 9, 10 and 11 to initiate functions on these boards. The data outputs are applied to the DATA OUT boards in Location No. 8.

There are two DATA OUT boards for serial operation, one for PHONE and one for TTY. Both boards contain the BIT OSCILLATOR circuitry for generating timing pulses, and a POWER ON PRE-CLEAR circuit for clearing certain flip-flops on the TIMING andCONTROL LOGIC board during turn-on. The DATA OUT-PHONE board may have either of two different BIT OSCILLATORS to produce two different read-out speeds.

Each of the boards contain circuitry used to determine that connection is made to the interface device. On the DATA OUT-PHONE board this is the PHONE LINE VALIDITY CHECK circuit and on the DATA OUT-TTY board it is the TELETYPE BUSY LIGHT INDICATOR circuit. The DATA OUT- PHONE board feeds directly to the interface device such as a data set or an acoustic coupler. The DATA OUT-TTY board feeds the TTY ADAPTER (connected to the output connector J15) which contains a relay used to open and close the loop teletypewriter circuit.

The FEED LOGIC board (Location No. 9) contains the circuitry used to recognize the request for a card feed, to initiate the signal to be fed to the solenoid to activate the card feed and to insure that one and only one card feed function is performed. Card feed may be initiated manually by the CARD FEED switch on the operator's panel or by a signal from the interface device. Either way, once the first card feed has been activated, the Motorola Document Reader will continue to feed cards until the last card in the hopper has been fed. Then another initiating signal is required in order to feed more cards.

The board in Location No. 10 contains the ALARM circuitry which is optional. These circuits are used to notify the operator of conditions that require the operator's attention. One of these options is HOPPER EMPTY which tells the operator that the last card has been fed and the hopper should be refilled if more data is to be transmitted.

The PHONE CONTROL boards (Location No. 11) are two boards, one for attended and one for unattended operation, used to recognize and initiate the "handshaking" signals that are required between the MDR and the interface device. These signals are used to indicate that all conditions are present that are required between the instruments for the transmission of data. The "handshaking" signals, some from the interface device and some from the MDR, are merely voltage levels and the circuits used recognize the required levels.

2. Parallel Operation (Refer to Figure 48)

As was mentioned earlier, parallel operation is very similar to serial operation. The differences are a different TIMING and CONTROL LOGIC board (Location No. 7), a different board in Location No. 8 (INTERFACE DRIVER) and a different board in Location No. 10 (READER CONTROL INTERFACE) and there is no board in Location No. 11.

The TIMING and CONTROL LOGIC board again uses the L.E., T.E. and FORMAT CLOCK signals to generate control signals that are applied to various other boards to initiate functions. There is a PARITY GENERATION circuit to generate a parity output if it is desired. This circuit is different from the one used for serial operation. Also PRE and POST CARD PROGRAM CODES are generated in much the same way. The primary difference lies in the fact that since timing is not needed, a BIT OSCILLATOR input is not needed and the output data is in parallel form, eliminating the need for a shift register. The data, being applied to input gates, is transferred to data output registers (R-S flip-flops). There is an output register for every data line in. One additional output, not found in serial operation, is a STROBE pulse which is fed to the interface device every time data is ready.

The INTERFACE DRIVER (Location No. 8) contains a driver circuit for every signal that is applied to the board. Their function is to provide

the level of signal required for the interface device. Since the operation is now parallel, all data must be present at the same time, hence the need for multiple driver stages. This board also contains a POWER ON PRE-CLEAR circuit, the same as the serial boards.

The READER CONTROL INTERFACE contains the circuitry for the initiation of functions such as MOTOR CONTROL and CARD FEED CONTROL. These circuits will be used much as the serial boards, that is, whenever signals and conditions between the Motorola Document Reader and the interface device are correct, then the MDR will be enabled to transmit data. The parallel board also contains an alarm function, the HOPPER EMPTY alarm circuit.

Although there will be no discussion, drawings on the MDR wiring for serial (Figure 49) and parallel (Figure 50) operation and cabling diagrams for serial (Figure 51) and parallel (Figure 52) operation are included to provide further information about the Motorola Document Reader. These will show all wiring and cabling and all connectors on the MDR. Refer to these drawings when the need arises to locate interconnections.

B. MASTER BOARDS (Refer to Figures 53 and 54)

There are two master boards, one for each serial operation and one for parallel operation. Each MASTER BOARD contains the sockets for the eleven Location boards and has the printed wiring for the interconnections between the various Location boards. Both boards have two end terminals for receiving connectors (P9 and P10) which contain all the wiring to the CARD CAGE. This comprises all of the inputs, outputs and voltages required for operation of the electronics contained in the Motorola Document Reader. The printed circuitry for the first six boards (Locations No. 1 through No. 6) remains the same for all practical purposes. Printed wiring for the last four boards (Locations No. 7 through No. 10) has changed slightly to accomodate the fact that different boards are used in Locations No. 7, 8 and 10.

Located at the top of each MASTER BOARD are several jacks and jumper wires. Each Document Reader has three* internally generated outputs or signals which are called program steps or program codes. The first two* signals (Program Codes No. 1 and No. 2) are generated as PRE-CARD codes. That is, they occur as the leading edge of the document enters the sensing area. The last signal (Program Code No. 3) is generated as the trailing edge of the document leaves the sensing area. These program codes are produced on the TIMING and CONTROL LOGIC Boards (Location No. 7 - Figures 68 and 69) and are available as jumper leads on the MASTER BOARD of the Card Cage. Program Code No. 1 is a WHITE control wire, Program Code No. 2 control wire is RED and No. 3 is BLACK.

Each of the control wires may be coded with up to ten** different codes. The ten codes are hardwired (not changeable) and available at colored jacks on the top edge of the Master Board. The codes that are available vary depending on the output language being used. The following table (Table 7) lists the jacks (in sequence as seen from the front of the unit) for the various languages. Refer to the legend for Table 5 for meanings of the codes.

*On the Parallel (8000 Series) Document Reader, only two signals are generated. These are a PRE-CARD code (a WHITE Control Wire) and a POST-CARD code (a BLACK Control Wire). An exception to this statement is in the case of a parallel (8000 Series), Hollerith to Hollerith, Document Reader. In this special case, there are no program codes.

**On numeric-only models, only four codes are available. These are NULL (NUL), CARRIAGE RETURN (CR), LINE FEED (LF) AND DELETE (DEL).

PROGRAM JACK	LANGUAGE			
COLOR CODE	USASCII-85 CHAR.	USASCII-15 CHAR.	PTTC/BCD	EBCDIC
CLEAR	NUL	NUL	--	--
WHITE	CR	CR	CR	CR
GREY	LF	LF	LF	LF
VIOLET	HT	--	HT	HT
BLUE	FF	--	--	UT
GREEN	DEL	DEL	DEL	DEL
YELLOW	US	--	--	US
ORANGE	FS	--	--	ETX
RED	GS	--	--	STX
BROWN	RS	--	EOB	RS

Table 7. Master Board Code Jacks

In addition, one code is wired directly from the TIMING and CONTROL LOGIC board to the DECODER boards. This code is BEL (called EOT in the PTTC/BCD code).

There are two paralleled jacks of each color except in the case of the clear jacks. Here, there are three paralleled jacks. This adds to the versatility by allowing the customer to use the same code more than once.

For example, a Line Feed (LF) may be desired at the beginning and at the end of a card. By plugging the WHITE control wire and the BLACK control wire into the paralleled Grey jacks, this would be accomplished. However, if the WHITE control wire and the RED control wire are plugged into jacks of the same color (other than the CLEAR jack), only one PRE-CARD code will be generated. In the case of the CLEAR (NUL) jacks, two NUL code characters will be generated.

The standard configuration for the program code control wires is: Program Code No. 1 (WHITE control wire) plugged into the WHITE (CR) jacks, Program Code No. 2 (RED control wire) plugged into the Grey (LF) jack and Program Code No. 3 (BLACK control wire) plugged into the Green (DEL) jack. However, no code plug combinations are forbidden.

C. SENSING HEAD (Refer to Figure 55)

In order to start it will be assumed that a card feed has been initiated in some manner--either by request from a remote device, by pressing the FEED switch on the operator's panel or by simply hand-feeding a card to the unit--and the card is starting to enter the DRIVE ROLLER area.

The sensing head area, prior to entrance of a card, is completely illuminated by light from the SENSOR LAMP ASSEMBLY. The SENSOR LAMP ASSEMBLY consists of 12 lamps, arranged in two parallel strings of six series lamps each. There are 15 phototransistors in the sensing head area, 12 for the data rows and one each for the FORMAT MARK, T.E. (Trailing Edge) and L.E. (Leading Edge). The phototransistors for the DATA ROWS and for the FORMAT MARK, as well as the phototransistors for the L.E. (Leading Edge) and T.E. (Trailing Edge), are in the standby state. As soon as the front edge of the card (or document) covers the phototransistors for the L.E. and T.E. (located under the surface of the read area), two signals are generated internally in the Document Reader. These signals are used as the PRE-CARD PROGRAM CODES. The exact generation of these codes will be covered during the analysis of the TIMING and CONTROL LOGIC BOARD.

Now, with both the L.E. and T.E. phototransistors covered by the card, the leading edge of the card has passed the data row phototransistors and the first column for data on the card is approaching the read area. The phototransistors are still illuminated by light reflected from the card and are at a LOW (0.0 Vdc to 0.5 Vdc) level.

Any data row that is marked in the first column of the card will diffuse the light reflected to that particular phototransistor. The light reflected to the FORMAT MARK phototransistor will also be diffused. The diffused light will cause the phototransistor to produce a change in signal from a LOW (0.0 Vdc to 0.5 Vdc) level to a HIGH (4.5 Vdc to 5.0 Vdc) level.

Therefore, for the first column of the card AND FOR EVERY MARKED COLUMN THEREAFTER, a HIGH (4.5 Vdc to 5.0 Vdc) level will be produced from the FORMAT MARK phototransistor and from the phototransistor associated with any marked DATA ROW.

D. SENSE AMPLIFIERS (Boards No. 1 and No. 2 Refer to Figures 56 and 57)

1. Data Row Sense Amplifiers (Refer to Figure 56)

Phototransistors that sense a mark on the card will apply a HIGH level signal to a SENSE AMPLIFIER corresponding to that data row. The 12 data row sense amplifiers are located on one board (Location No. 1). All 12 amplifiers are identical. One common potentiometer is used to adjust the sensitivity of all amplifiers.

The HIGH level input to the sense amplifier is applied to the base of the input transistor (Q25 - Q36). The base of the input transistor is controlled at a point such that the transistor is normally conductive. The control is accomplished by transistor Q1-Q12 and transistor Q13-Q24. The base of transistor Q13-Q24 is tied to the potentiometer R73 which determines the base voltage of the transistor. This in turn controls the conduction of transistor Q13-Q24 which sets the base voltage of transistor Q1-Q12. As was mentioned earlier, the voltage on the base of transistor Q25-Q36, determined by the conduction of transistor Q1-Q12, is such that Q25-Q36 is normally conducting. As a result of transistor Q25-Q36 conducting, the base of transistor Q37-Q48 is positive, transistor Q37-Q48 is conducting and the output of the sense amplifier is LOW or near ground potential.

When the HIGH level input arrives from a phototransistor, the base of transistor Q25-Q36 becomes more positive, Q25-Q36 becomes cutoff and its collector potential approaches ground. This causes the base of transistor Q37-Q48 to become less positive, cutting off the transistor, and its collector potential becomes more positive. The resultant is a HIGH level output from the sense amplifiers for a HIGH level input from the phototransistor.

After a time period determined by capacitor C1-C12 which was charged more negative as a result of the HIGH level input, the base of Q25-Q36 again reaches a potential which allows Q25-Q36 to conduct, the base of transistor Q37-Q48 becomes more positive, transistor Q37-Q48 conducts and the output of the sense amplifier is again a LOW level output.

2. Format Mark, L.E. and T.E. Sense Amplifiers (Refer to Figure 57)

When the Format Mark phototransistor senses a mark (which it will do for every data column)

and when the L.E. and T.E. phototransistors sense the leading edge of a card, a HIGH (4.5 Vdc to 5.0 Vdc) level signal will be applied at the input of their respective sense amplifer. These sense amplifiers are located on one board (Location No. 2) and perform the same function as the data row sense amplifiers; that is, upon receipt of a HIGH level signal, each of the three sense amplifiers will produce a HIGH level signal in their output. Unlike the data row sense amplifiers, however, each amplifier has its own sensitivity control.

The format mark sense amplifier is very similar in operation to the data row sense amplifiers. An input signal, arriving at the base of transistor Q3 turns off the transistor. The transistor's collector and the base of transistor Q4 will become less positive and transistor Q4 will cut off. This results in the collector of Q4 and the collector of Q5 becoming more positive, driving Q5 into conduction. The collector of Q5 is now near ground potential. This LOW level signal is applied to a gate and the inverted output of the gate becomes a HIGH level signal output.

The potential on the base of Q3 is controlled by Q1 which is controlled by Q2 which in turn is controlled by the setting of R3, the sensitivity control for the format mark sense amplifier. Capacitor C2 is the component that determines the maximum width of the output pulse.

The L.E. (Leading Edge) and T.E. (Trailing Edge) sense amplifiers are identical and operate in the same manner. As the HIGH level signal is received from the phototransistor, capacitor C4 (C6) has to charge. Its charge path through R12, CR6 and CR4 (R18, CR12 and CR10) results in a more positive voltage on the base of transistor Q6 (Q8). Transistor Q6 (Q8) conducts and its collector becomes less positive along with the base of Q7 (Q9). Transistor Q7 (Q9) is cut off and its collector potential becomes more positive, producing a HIGH level output.

As the input signal returns to a LOW (0.0Vdc to 0.5Vdc) level, the junction of C4 (C6) and CR4 (CR10) tries to swing negative. The point is clamped by CR2 (CR8) to a maximum negative voltage of -0.7 Vdc. At this time, transistor Q6 (Q8) is cut off, the collector of Q6 (Q8) and the base of transistor Q7 (Q9) move positive and transistor Q7 (Q9) turns on producing a LOW level output from the sense amplifier. Diodes CR1, CR3 and CR5 (CR7, CR8 and CR11) provide a discharge path for capacitor C4 (C6).

The outputs from the sense amplifiers are applied to the TIMING and CONTROL LOGIC BOARD (Location No.7).

E. DATA REGISTER (Refer to Figure 58)

The data register receives a HIGH (4.5 Vdc to 5.0 Vdc) level input from the sense amplifiers whose phototransistors have sensed data. The input from the sense amplifier is to one input of an AND gate designated the INPUT DATA GATE. There are 12 INPUT DATA GATES. The other input is common to all the input data gates and is the GATED CLOCK (Window) signal. The GATED CLOCK (Window) signal is derived from the format mark or clock signal and is a HIGH (4.5 Vdc to 5.0 Vdc) level signal.

With two HIGH level inputs to any INPUT DATA GATE receiving a signal from a sense amplifier, the requirements for the AND gate are satisfied and an inverted output or LOW is produced. The LOW is inverted and applied to two AND gates. One AND gate is from a group of 12 gates designated as CARD gates. The other AND gate is found in the group of gates called PAGE gates.

The PAGE and CARD gates permit both cards (and pages) with a normal format and pages with an inverted format to be read equally well by the Document Reader. Either the CARD or PAGE group receives a HIGH (+12.0 Vdc) level signal whenever the PAGE-CARD switch on the operator's panel is placed in that particular position. The other HIGH (4.5 Vdc to 5.0 Vdc) level signal for the AND gate is provided from the outputs of the inverters.

Whichever CARD gate (or PAGE gate) receives two HIGH inputs will produce an inverted or LOW (0.0 Vdc to 0.5 Vdc) output. The outputs of the PAGE gates and the CARD gates are cross-connected. That is, the output of the PAGE gate associated with data row "12" is connected to the output of the PAGE gate associated with data row "9", data row "11" (CARD) to data row "8" (PAGE,) data row "0" (CARD) to data row "7" (PAGE), etc.

The DATA REGISTER FLIP-FLOPS (one for each data row) are at present in the RESET condition. They are placed in this condition by a D.C. REGISTER (clear) signal. The D.C. REGISTER (clear) signal is a LOW (0.0 Vdc to 0.5 Vdc) level signal and is generated by the TIMING and CONTROL LOGIC board to clear the DATA REGISTER either after the data in the flip-flops has been recognized or when the end of a card is clearing the sensing area. In the RESET condition, the "1" output is LOW and the "0" output is HIGH. There are two outputs from every flip-flop providing 24 signals for coding purposes. The cross-connected outputs from the CARD and PAGE gates are applied to the SET input of the DATA REGISTER FLIP-FLOPS.

If a DATA REGISTER flip-flop receives a LOW level signal from either a PAGE or CARD gate, that flip-flop will SET or change state. At that time, the "1" output will be HIGH (4.5 Vdc to 5.0 Vdc) and the "0" output will be LOW (0.0 Vdc to 0.5) Vdc). If only one set signal is present (that is, only one data row has information marked), that flip-flop will have a HIGH "1" output and a LOW "0" output and the other 11 flip-flops will have LOW "1" outputs and HIGH "0" outputs. All 24 outputs from the DATA REGISTER flip-flops are applied to the DECODER boards (Location No. 4, No. 5 and No. 6, if used).

F. DECODER BOARDS (Refer to Figures 59 to 67)

An earlier section referred to the various output languages or codes that are available as Motorola Document Reader outputs. In order to produce these codes, the input code (Hollerith) must be processed and encoded. This processing occurs on the decoder boards,

located in Positions No. 4, No.5 and No. 6 of the Card Cage.

The most common output language is USASCII-85 character. However, all of the other output codes --USASCII-15 character, PTTC/BCD and EBCDIC-- are used. The encoding process for each code is covered in the following paragraphs.

1. USASCII-85 Character (Refer to Figures 59, 60 and 61)

   Three decoder boards are used to mount the gates used for decoding and encoding the 85 recognized Hollerith marked characters of the USASCII code. Each board receives inputs from the outputs of the DATA REGISTER flip-flops. The inputs are both HIGH and LOW signals. Board No. 4 receives all 24 outputs of the DATA REGISTER flip-flops. Board No. 5 receives 15 of the outputs of the DATA REGISTER flip-flops, plus three inputs from Board No.4. These inputs are three special signals generated on Board No. 4. Board No. 6 receives 15 of the outputs of the DATA REGISTER flip-flops, two of the three special signals from Board No. 4 and two signals generated on Board No. 5 for a total of 19 inputs.

   All the inputs are connected to input AND gates designated as DECODER GATES. There are a total of 90 DECODER GATES. This Total includes one for each character (85), one gate for space, one for each special signal or code (3) and one gate used to recognize the EJECT code. Since each character has its own gate, the inputs to the three boards are connected to the gate of the particular character for which that input is needed.

   NOTE

   Although both HIGH and LOW level signals are received at the inputs to the decoder boards, all inputs to any gate must be HIGH to activate that gate.

   When an input DECODER gate receives the proper inputs and is activated, a LOW (0.0 Vdc to 0.5 Vdc) level signal is produced in its output. The LOW level signal DECODER gate output is applied either directly to ENCODER gate inputs or through INVERTER and BUFFER AMPLIFIERS (for isolation) to ENCODER gate inputs.

   There are seven ENCODER gates (OR gates), one for each information bit of the USASCII code. The inputs of the seven gates are matrixed with the outputs of the 85 character DECODER gates (either directly or after passing through the INVERTERS and BUFFER AMPLIFIERS). Any input DECODER gate that has sensed a character will in turn feed a LOW level input to the proper ENCODER gates. The outputs of those ENCODER gates receiving a LOW level input will be a HIGH (4.5 Vdc to 5.0 Vdc) level signal.

   The seven ENCODER gates outputs are supplied to the TIMING and CONTROL LOGIC board (Location No. 7).

   Earlier in this discussion, mention was made of three special signals generated on Board No. 4 and two special signals generated on Board No. 5. These signals are as follows:

   Board No. 4

   - (a) - Generated any time that data is not marked in data rows "12", "11" and "0".
   - (b) - Generated anytime that data is not marked in data rows "1", "2", "3", "4", "5", "6", "7", "8" and "9".
   - (c) - Generated any time that data is not marked in data rows "3", "4", "5" and "7".

   Board No. 5

   - 8 - Generated any time that data is not marked in data row "8".
   - $\bar{8}$ - Generated any time that data is marked in data row "8".

   In addition to the above, other inputs and outputs should be mentioned. These are as follows:

   Board No. 4

   - EJECT - Generated by marking data rows "12" and "11" in the same column. Provides a faster transporting of the card after data has been sensed. (The DECODER gate for EJECT also receives an input from GATED CLOCK (Window). This would prevent an eject from occuring due to a MARK condition in data rows "12" and "11" when a FORMAT MARK was not present.)
   - US (UNIT SEPARATOR) - An output control code sent to an interface device to initiate a function at the interface device. The signal may be generated by marking data rows "11" "9", "8" and "7" or initiated by the use of a program code control wire.
   - RS (RECORD SEPARATOR) - An output control code sent to an interface device to intiate a function at the interface device. The signal may be generated by marking data rows "11", "9", "8" and "6" or initiated by the use of a program code control wire.
   - GS (GROUP SEPARATOR) - An output control code sent to an interface device to initiate a function at the interface device. The signal may be generated by marking data rows "11", "9", "8" and "5" or initiated by the use of a program code control wire.
   - FS (FILE SEPARATOR) - An output control code sent to an interface device to initiate a function at the interface device. The signal may be generated by marking data rows "11", "9", "8" and "4" or initiated by the use of a program code control wire.
   - RUBOUT - An output signal (also called

DELETE) used as an indication to the interface device for timing and control functions. The signal may be generated by marking data rows "12", "9" and "7" or initiated by the use of a program code control wire.

- SHIFT - A special function, used with the USASCII decoder boards, enables all characters of the USASCII code to be used (refer to figure 62). By marking data rows "11" and "0" and marking the USASCII Code in data rows "1" through "7", all 128 USASCII codes can appear in the output, when marked on the card. A special board is used in Location No. 4 when SHIFT is incorporated.

All explanations for the USASCII-85 character decoding remain valid when SHIFT is added. However, the seven ENCODER gates no longer feed to the TIMING and CONTROL LOGIC board (Location No. 7). The SHIFT board contains additional SHIFT and DECODER GATES and INVERTERS plus an AND gate (DECODER gate) to detect the marked SHIFT code.

Upon detection of a SHIFT code (data rows "11" and "0" marked), the LOW level signal DECODER gate output is applied as a common input to seven output DECODER gates. Each output DECODER gate receives its other input from one ENCODER gate. Since a LOW level signal is being applied by the SHIFT DECODER gate, these output DECODER gates are blocked and will not produce a proper output.

However, tied in parallel to the output DECODER gates receiving inputs from the ENCODER gates are seven SHIFT gates whose input is directly from the DATA REGISTER flip-flops for data rows "1" through "7". The second input to these AND gates is an inverted output of the SHIFT DECODER gate. Each gate for which data was marked now has two HIGH level inputs and produces an inverted (LOW) output.

Thus when SHIFT is recognized, the seven output DECODER gates are disabled and the seven SHIFT gates are enabled.

The LOW level outputs (where applicable) of these seven SHIFT gates, applied to the inputs of INVERTERS, produce HIGH level outputs from the INVERTERS. These outputs are now applied to the TIMING and CONTROL LOGIC board.

NOTE

The SHIFT function was not included in initial production of decoder board No. 4 - USASCII-85 Character.

Board No. 5

- ? - The code is normally generated by the marking of data rows "0", "8" and "7". However, the code could be sent to the interface device by inserting a LOW level signal on the indicated pin.

- SPACE SET - This signal is generated by a flip-flop on the TIMING and CONTROL LOGIC board and provides a HIGH level signal into Board No. 5. The input is one input to an AND gate. The other inputs are (a) and (b) and is used to decode the fact that a space is present on the document.

2. USASCII - 15 Character (Refer to Figure 63)

Only one decoder board is used for 15 Character USASCII. This board is placed in Location No. 4. The characters that are recognized are numerals "0" through "9", space and four program codes, DEL (Delete), LF (Line Feed), CR (Carriage Return) and BEL. Only the numerals or space are marked on the document to be read. The program codes are wired into the master board. All other characters are invalid. EJECT is still recognized by the Document Reader but, of course, this code is not transmitted.

Inputs to the board are as follows:

- Both "1" and "0" outputs of the DATA REGISTER flip-flops for data rows "0" through " "9".

- The "1" output of the DATA REGISTER flip-flops for data rows "11" and "12".

- GATED CLOCK (Window) from the TIMING and CONTROL LOGIC board

- SPACE SET from the TIMING and CONTROL LOGIC board.

- DEL, LF and CR as connected by the program code control wires from jacks on the master board.

- BEL from the BEL flip-flop on the TIMING and CONTROL LOGIC board.

Outputs from the board are as follows:

- EJECT is applied to the EJECT flip-flop on the TIMING and CONTROL LOGIC Board to initiate a CARD EJECT and a CARD FEED.

- Seven LINE OUT outputs, one for each bit of USASCII information.

- CARD FEED INHIBIT is connected to the CARD FEED output from the TIMING and CONTROL LOGIC board to prevent a card feed after an invalid character.

The inputs from the DATA REGISTER flip-flops are to DECODER gates. There are ten expanded input AND gates (data rows "0" through "9"), one expanded input AND gate for SPACE and one AND gate for EJECT. Any valid code will produce a LOW level output from its gate. This in turn produces a HIGH at jumper J1.

NOTE

Determine from the board the position of the jumpers and observe the notes on Figure 63 as to the results of the different jumper positions.

As long as a valid code is marked on a document an AND gate (to the left of the "SPACE SET" AND gate) will supply the ENCODER gate for lines "5" and "6" with a LOW level signal. This produces a HIGH level output on lines "5" and "6". Any other ENCODER gates (if needed for the USASCII code) will be supplied with a LOW level signal directly from the "0" output of the DATA REGISTER flip-flop corresponding to the marked data row. This result in HIGH level outputs on the lines needed to produce the correct USASCII code.

If a space is desired, the gate previously mentioned (to supply a LOW to ENCODER gates "5" and "6") will not be used (its output is now HIGH). Instead the "SPACE SET" AND gate, with both its inputs HIGH, will supply a LOW level signal to ENCODER gate "6". This produces a HIGH on line "6" which is the only line that needs to be HIGH to correspond to the USASCII code for SPACE.

When an invalid code is marked, a LOW level signal appears at the right side of jumper J1 (either through J1 or J3). The LOW level signal activates the INVALID CHARACTER CARD FEED INHIBIT circuit. When activated this circuit produces a LOW level output which prevents another card feed from being initiated. The invalidly marked card, being the last card through the sensing area, may now be corrected. The Document Reader now must be manually operated to again start cards feeding automatically.

Once card feed is initiated again, the INHIBIT circuit is reset by the first program step (DEL, CR or LF) connected by Jumper J5.

3. PTTC/BCD-64 Character (Refer to Figure 64)

One decoder board (Location No. 4) contains the gates decoding and encoding the 64 recognized Hollerith marked characters of the PTTC/BCD code. Inputs to the decoder board are as follows:

- Both the "1" and "0" outputs of the DATA REGISTER flip-flops for data rows "1" through "9".
- The "1" output of the DATA REGISTER flip-flops for data rows "0", "11" and "12".
- GATED CLOCK (Window) from the TIMING and CONTROL LOGIC board.
- DEL, EOB (End of Block), HT (Horizontal Tabulation), CR and LF as connected by the program code control wires from jacks on the master board.
- EOT (End of Transmission) from the BEL flip-flop on the TIMING and CONTROL LOGIC board.

Outputs from the board are as follows:

- EJECT is applied to the EJECT flip-flop on the TIMING and CONTROL LOGIC board to initiate a CARD EJECT and a CARD FEED signal.
- Six LINE OUT outputs, one for each bit of PTTC/BCD information.

Most decoder board inputs are applied to input DECODER gates ensuring proper recognition of the marked signals. However, some inputs are applied directly to the ENCODER gates. Either way, all marked codes from the documents provide inputs that are either matrixed into input DECODER gates which, when all inputs are proper apply LOW level signals to the ENCODER gates or are applied directly as LOW level signals to the ENCODER gates.

The ENCODER gates (six gates, one for each PTTC/BCD information bit) are expanded input OR gates. Each ENCODER gate requires only one LOW level input to produce a HIGH level output. Any ENCODER gate receiving a LOW level input feeds a HIGH level output to the output DECODER gates. One input of the DECODER gates (common to all six gates) is normally at a HIGH level. When both DECODER gate inputs are HIGH, a LOW level output is produced. This LOW level signal is now inverted and becomes a HIGH level signal on the LINE OUT.

When the SHIFT function is used (data rows "11" and "0" marked), an input DECODER gate is activated and produces a LOW level signal. The common input to the six output DECODER gates is now LOW. This prevents inputs from the ENCODER gates from activating the output DECODER gate. However, the output of the SHIFT DECODER gate is also inverted and applied as a HIGH input to six SHIFT gates. Data columns marked for the SHIFT function (data rows "11" and "0") and with PTTC/BCD codes marked in data rows "$\overline{1}$" through "6" produce HIGH inputs to the SHIFT gates. Those SHIFT gates that are activated produce LOW level signals. The SHIFT gates are parallelling the output DECODER gates. Therefore, the LOW level outputs from the SHIFT gates are applied to the INVERTERS and a HIGH level signal appears on the LINE OUT outputs. The six LINE OUT outputs are applied to the TIMING and CONTROL LOGIC board.

When the SHIFT function is used, all 72 characters of the PTTC/BCD code may be marked on the document and produced in the output.

4. EBCDIC-159 Character (Refer to Figures 65 and 66)

The circuitry in decoding the Hollerith code and encoding into the EBCDIC code is contained on two decoder boards. A total of 150 EBCDIC characters may be marked on documents in the Hollerith code. When the SHIFT function is initiated by marking data rows "11" and "0" on the document, all 256 characters of the EBCDIC code may be marked on the documents in data rows "1" through "8", recognized by the decoder boards and transmitted to the interface device.

(a.) Board No. 1 (Location 4) (Refer to Figure 65)

Board No. 1 used for the EBCDIC code receives

- Both the "1" and "0" outputs of the DATA REGISTER flip-flops for all data rows.
- GATED CLOCK (Window) from the TIMING and CONTROL LOGIC board.
- 5 LINE, 6 LINE, 7 LINE and 8 LINE from their respective ENCODER gates on Board No. 2 (Location No. 5)
- US, RS, CR, VT, DEL, LF, HT, ETX (End of Text) and STX (Start of Text) as connected by the program code control wires from jacks on the master board.
- BEL from the BEL flip-flop on the TIMING and CONTROL LOGIC board.

Outputs from Board No. 1 (EBCDIC) are as follows:

- EJECT is applied to the EJECT flip-flop on the TIMING and CONTROL LOGIC board to initiate a CARD EJECT and a CARD FEED signal.
- Outputs from the "0" output of the DATA REGISTER flip-flops for data rows "0", "11" and "12" coupled to EBCDIC Board No. 2 (Location No. 5).
- (a), N, and N" functions generated by special grouping of inputs from the DATA REGISTER flip-flops on Board No. 1 and applied to EBCDIC Board No. 2 (Location No. 5).
- $\overline{N}$, $\overline{N'}$, and $\overline{N''}$ inverted outputs of N, N' and N" respectively applied to EBCDIC Board No. 2 (Location No. 5).
- Eight LINE OUT outputs, one for each bit of EBCDIC information.

DATA REGISTER flip-flop outputs are applied to either the ENCODER gates directly, to input DECODER gates which in turn apply signals to the ENCODER gates or to input DECODER gates to generate the special functions (a), N, N', N". Special functions (groupings of inputs) generated on Board No. 1 are generally used on Board No. 2 (Location No.5) and the outputs of these gates are applied to Board No. 2.

The remaining input DECODER gates produce LOW level outputs upon receipt of proper inputs and apply these LOW level signals to the inputs of the ENCODER gates. The ENCODER gates, upon receipt of a LOW level signal, produce a HIGH level output which is applied to one input of the output DECODER gates. The other input of all eight output DECODER gates is common and is the output of the input DECODER gate responding to the SHIFT code (data rows "11" and "0" marked). As long as the SHIFT function has not been marked and recognized, the output of the gate is high. This output enables the output DECODER gates. Whichever DECODER gate is receiving an input from an ENCODER gate will produce a LOW level signal in its output. This signal is inverted and becomes a HIGH level signal on the LINE OUT output.

When the shift function is used by marking data rows "11" and "0" on the document, all 256 characters of the EBCDIC code may be marked in data rows "1" through "8" on the document. When the SHIFT input DECODER gate receives inputs generated by marking data rows "11" and "0", its output goes LOW. This LOW is applied to the common input of the output DECODER gates disabling them. At the same time, an output of the SHIFT input DECODER gate is inverted to HIGH and applied to one input of all eight SHIFT gates. When any row of data rows "1" through "8" are marked, the corresponding SHIFT gate will produce a LOW level signal in its output. The outputs of the SHIFT gates are tied in parallel with the outputs of the output DECODER gates. They provide inputs to the INVERTERS. The LOW level output of the SHIFT gates is inverted and becomes a HIGH level signal on the LINE OUT outputs. The eight LINE OUT outputs are applied to the TIMING and CONTROL LOGIC board.

(b.) Board No. 2 (Location No. 5) Refer to Figure 66)

Board No. 2 used for the EBCDIC code receives the following inputs:

- Both the "1" and "0" outputs of the DATA REGISTER flip-flops for data rows "9", "8" and "1".
- The "1" output of the DATA REGISTER flip-flops for data rows "2", "0", "11" and "12".
- The "0" output of the DATA REGISTER flip-flops for data rows "0", "11", and "12" coupled from EBCDIC Board No. 1 (Location No. 4.)
- $\overline{N}$, $\overline{N'}$ and $\overline{N''}$ inverted outputs of special functions N, N' and N" respectively from EBCDIC Board No. 1 (Location No. 4).
- SPACE SET from the TIMING and CONTROL LOGIC board.

Outputs from Board No. 2 (EBCDIC) are as follows:

- 5 LINE, 6 LINE, 7 LINE and 8 LINE, decoded and encoded on Board No. 2, and applied to Board No. 1 (Location No. 4).

All inputs to Board No. 2 are inputs to DECODER gates. The inputs and the outputs are matrixed to accomplish recognition of the desired codes. The outputs of the DECODER gates are LOW level outputs when all inputs are proper (HIGH). The gates that are activated supply LOW level inputs to ENCODER gates. The ENCODER gates produce a HIGH level output when activated. Only 5 LINE, 6 LINE, 7 LINE and 8 LINE are encoded on this board. The HIGH level outputs from the ENCODER gates are applied to the inputs of ENCODER gates on EBCDIC Board No. 1 (Location No. 4).

5. Parallel Operation

All of the codes mention above -- USASCII-86 character, USASCII-15 character, PTTC/BCD and EBCDIC -- may be operated in the serial or parallel mode of operation. There is no difference in the connections or the decoding/encoding process. The decoder boards remain the same. The differences between a serial and a parallel Document Reader are:

- A serial and a parallel Master Board
- A serial and a parallel TIMING and CONTROL LOGIC board.
- A serial DATA OUT-PHONE board (Location No. 8) and a parallel INTERFACE DRIVER board.
- A serial ALARM-BEL or HOPPER EMPTY board (Location No. 10) and a parallel READER CONTROL INTERFACE board.

Operation of the Document Reader remains basically the same. However, the information to the interface device is now in parallel form instead of serial form. This is accomplished by the different TIMING and CONTROL LOGIC board.

When a parallel Document Reader is used, one additional output language is available. This language is Hollerith (refer to Figure 67). A special decoder board (Location No.4) receives the outputs from the "1" outputs of the DATA REGISTER flip-flops for data rows "12," "11", and "2" through "9". The inputs are all HIGH level inputs. The HIGH level inputs for data rows "12" and "11" are applied to the only DECODER gate on the board. This gate recognizes the EJECT code. A third input to the gate is from GATED CLOCK (Window). When all three inputs are present, the output becomes LOW and the signal is applied to the EJECT flip-flop on the TIMING and CONTROL LOGIC board.

The data rows "2" through "9" inputs are wired straight throught the board and are input signals to the TIMING and CONTROL LOGIC board.

The "1" outputs of the DATA REGISTER flip-flops for data rows "1" and "0" are wired directly from the DATA REGISTERS (Location No. 3) to the TIMING and CONTROL LOGIC board (Location No. 7.)

Any code marked in Hollerith on the document will be transmitted to the interface device in the Hollerith code.

G. TIMING AND CONTROL LOGIC BOARDS (Refer to Figures 68 and 69)

Most of the control functions are either generated on this board (Location No.7) or outputs from the board initiate the function. There are two TIMING and CONTROL LOGIC boards, one for serial and one for parallel mode of operation.

1. Serial Operation (Refer to Figure 68)

Inputs to this board are as follows:

- L.E. and T.E. from the Leading Edge and Trailing Edge Sense Amplifiers.
- FORMAT CLOCK from the Format Clock Sense Amplifier.
- EJECT from the DECODER board (Location No. 4).
- BEL (IN) from the circuit (Location No. 10) that recognizes when the last card has left the hopper.
- BIT OSCILLATOR from the oscillator (Location No. 8) used to generate the timing clock pulses.
- POWER ON PRE-CLEAR from the circuit (Location No. 8) used to clear circuits when power is first applied.
- DATA LINES which are receiving the outputs from the decoder boards. There may be six, seven or eight DATA LINES depending on the code to be used.

Outputs from the TIMING and CONTROL LOGIC board are as follows:

- CARD FEED used to initiate the mechanical function of transporting a card forward to the sensing area.
- DATA REGISTER (CLEAR) used to insure the DATA REGISTERS (Location No. 3) are reset (clear) and ready to receive new data.
- SPACE SET applied to the DECODER boards to recognize that a space is present when no data rows are marked on the document (only a FORMAT MARK)
- GATED CLOCK (Window) used to signal all gates as to the time when DATA should be read.
- GATED CLOCK (Logic) used to signal circuits (Locations No. 10 and No. 11) that a card is in the process of being read.
- BEL (OUT) applied to the DECODER boards to initiate and transmit a BEL code when the last card has left the hopper.
- PROGRAM STEP 1 actuated by the leading edge of the document and used to transmit a control code to the receiving terminal.
- PROGRAM STEP 2 also actuated by the leading edge of the document. Provides a second control function (if desired) at the receiving terminal.
- PROGRAM STEP 3 actuated by the trailing edge of the document. Transmitted to the receiving terminal to perform a control function.

- SERIAL DATA (OUT) applies the serial bit information to the DATA LINE DRIVER (Location No. 8) to feed the interface device.

As the leading edge of the document covers the L.E. phototransistor, a HIGH level signal is applied to one input of a gate at the input of the L.E. PROGRAM CONTROL CHARACTER REGISTER. The other input is HIGH at the moment producing a momentary LOW at the gates input. This triggers the RS flip-flop producing a HIGH from its "1" output. This HIGH is inverted to a LOW Level signal called PROGRAM STEP 1. This signal is applied to the DECODER boards to encode the character that has been selected from the jacks located on the MASTER BOARD. This character is now present on the LINE OUT outputs from the DECODER boards.

When the gate on the input of the L.E. PROGRAM CONTROL CHARACTER REGISTER went LOW momentarily, the "0" PRESET REGISTER was triggered. Its output, applied to an AND gate, clears the SHIFT REGISTER and sets "0" in all the J-K flip-flops (except for the first which will remain in the "1" condition and the second which will be set direct in the "1" condition).

After the "0" PRESET REGISTER (a one-shot multivibrator) times out, the DATA XFER ENABLE will be activated. Both outputs from the DATA XFER ENABLE one-shot will be used. The "1" output is HIGH and is common input to all the DATA INPUT gates. Any gate having DATA on its input will produce a LOW output and set its respective J-K flip-flop of the SHIFT REGISTER. The "0" output of the DATA XFER ENABLE will activate the TRIGGER ENABLE.

The board in Location No. 8 contains the BIT OSCILLATOR which is a free-running multivibrator. Its output has been blocked by the TRIGGER ENABLE circuit. When the TRIGGER ENABLE is activated, the signal from the BIT OSCILLATOR can now toggle the TRIGGER ENABLE output gates. The output gates feed all the J-K flip-flops of the SHIFT REGISTER and the input to the ÷ 10 counter. Every time the BIT OSCILLATOR input goes LOW, the J-K flip-flops are triggered and any DATA set in the J-K flip-flops will be shifted serially to the last J-K and through the SERIAL DATA gate to the DATA LINE DRIVER (location No. 8)

While the SHIFT REGISTER data is being shifted, the COUNTER has been counting the number of input pulses. On the second input, an output from the counter is fed through inverters and gates and become the DATA REGISTER (CLEAR) signal.

Since the data has already been decoded, encoded and set in J-K flip-flops of the SHIFT REGISTER, the DATA REGISTERS may be cleared to prepare for the next character. On the eighth input, an output from the COUNTER feeds a trigger to the J-K flip-flop in the L.E. PROGRAM CONTROL CHARACTER REGISTER. This causes the "1" output of this flip-flop to go LOW. This LOW signal becomes PROGRAM STEP 2 and is again used to initiate a character previously selected from the jacks on the MASTER BOARD. This is PRE-CARD PROGRAM CODE 2. The character will be set in the ENCODER gates on the DECODER boards.

On the ninth input to the counter, an output is applied to gates to AND with the output of the PARITY GENERATOR. PARITY (a check for correct code) may be ODD, EVEN or not used at all depending on the usage. The PARITY GENERATOR, which starts off in a SET condition receives a toggle derived from the BIT OSCILLATOR and an input from a J-K flip-flop in the SHIFT REGISTER. Every time the toggle goes LOW and the input from the SHIFT REGISTER is HIGH, the PARITY GENERATOR changes state. This enables the PARITY GENERATOR to provide a signal to add a bit to the output if it is needed.

On the tenth input to the counter, several actions occur. First, the output of the counter triggers the END OF CHARACTER RESET multivibrator. The "0" output goes LOW and (1) SETS the PARITY GENERATOR, (2) deactivates the TRIGGER ENABLE and (3) SETS the TRAILING EDGE PROGRAM CONTROL CHARACTER FLIP-FLOP.

The "1" output of the END OF CHARACTER RESET circuit goes HIGH and adds with the "0" output (HIGH) as inputs to an AND gate which results in the "0" PRESET REGISTER being triggered again. This of course starts the cycle again of transferring data to the SHIFT REGISTER, enabling the BIT OSCILLATOR outputs and starting the ÷ 10 COUNTER again. The character that was placed in the ENCODER gates of the DECODER boards by PROGRAM STEP 2 will now be transmitted to the interface device.

The "1" output from the END OF CHARACTER RESET circuit also resets the L.E. PROGRAM CONTROL CHARACTER REGISTER R-S flip-flop and the BEL flip-flop.

The above has described the sequence of events as a document has entered the sensing area and the two PRE-CARD PROGRAM CODES have been generated. Now, as the document progresses through the sensing area, the data columns must be read. Each column has a FORMAT MARK. This mark is sensed and amplified and applied to the TIMING and CONTROL LOGIC board. Every time a signal appears as a result of a FORMAT MARK, the "0" PRESET REGISTER will be triggered and data will be transferred to the SHIFT REGISTER, the BIT OSCILLATOR will shift the data out serially and the ÷ 10 COUNTER will keep the proper timing. At the end, the sequence will be stopped by the END of CHARACTER RESET. These portions of the TIMING and CONTROL LOGIC board remains essentially the same whether it is reading the data columns or reading the program codes.

The FORMAT MARK will also cause generation of GATED CLOCK (Window), GATED CLOCK (Logic) and SPACE SET. These signals are used for timing to determine if data is present and to encode for special conditions.

The EJECT circuit will, upon recognition of an

EJECT code actuate a CARD FEED and the card will be transported through the reading area more rapidly. This enables faster reading of cards that do not contain data for the entire column area. However, no card may be ejected before column 24 on an 80-column card (Column 12 on a 40-column card).

As the L.E. phototransistor is uncovered by the trailing edge of the document, the END OF CARD gate is activated and a CARD FEED is initiated to cause another card to be started (only in automatic feed models). Then when the T.E. phototransistor is uncovered by the trailing edge of the document, the TRAILING EDGE PROGRAM CONTROL CHARACTER flip-flop is triggered and its "1" output goes LOW. This signal is the PROGRAM STEP 3 output and the character that was placed in the ENCODER gates of the DECODER boards, selected from the jacks located on the MASTER BOARD, will now be transmitted.

Finally, the output of the LOGIC CLEAR gate will clear the +10 COUNTER and set the "0" outputs of the last two J-K flip-flops of the SHIFT REGISTER to a HIGH level condition. As the next document arrives at the sensing area, the sequence will start again.

2. Parallel Operation (Refer to Figure 69)

Inputs to this board are as follows:

- L.E. and T.E. from the Leading Edge and Trailing Edge Sense Amplifiers.
- FORMAT CLOCK from the Format Clock Sense Amplifier.
- EJECT from the DECODER board (Location No. 4).
- PARITY INHIBIT from the DECODER board (Location No. 4) to prevent a PARITY signal from being generated. (Only used with an EBCDIC code.)
- EXTERNAL STROBE RESET received via Location No. 8 board (INTERFACE DRIVER) from the interface device to reset the STROBE GENERATOR flip-flop.
- EXTERNAL DATA LINE RESET received via Location No. 8 board (INTERFACE DRIVER) from the interface device to reset the OUTPUT DATA flip-flops.
- POWER ON PRE-CLEAR from the circuit (Location No. 8) used to clear circuits when power is first applied.
- DATA LINES which are receiving the outputs from the decoder boards. There may be six, seven, eight or twelve DATA LINES depending on the code to be used.

Outputs from the TIMING and CONTROL board are as follows:

- CARD FEED used to initiate the mechanical function of transporting a card forward to the sensing area.
- END OF CARD PULSE sent to the interface driver to indicate that the end of a card has cleared the sensing area.
- DATA REGISTER (clear) used to insure the DATA REGISTERS (Location No. 3) are reset (clear) and ready to receive new data.
- GATED CLOCK (Window) used to signal all gates as to the time when DATA should be read.
- SPACE SET applied to the DECODER boards to recognize that a space is present when no data rows are marked on the document (only a FORMAT MARK).
- START of RECORD (PROGRAM STEP 1) actuated by the leading edge of the document and used to transmit a control code to the receiving terminals.
- END of RECORD (PROGRAM STEP 2) actuated by the trailing edge of the document. Transmitted to the receiving terminal to perform a control function.
- STROBE transmitted to the receiving terminal as an indication that data may be read.
- LINE OUT are the data lines providing outputs to the DATA LINE DRIVERS (Location No. 8). Six, seven, eight or twelve lines may be used depending on which code is used.

As the leading edge of a document covers the L.E. phototransistor, a HIGH level signal is applied to one input of a gate feeding the L.E. PROGRAM CODE flip-flop. The other input to the gate is HIGH and a momentary LOW is produced at the gate output. This LOW signal activates the R-S flip-flop and its "1" output goes HIGH. This HIGH level signal is applied to an inverter and fed out as a LOW level signal. This is START of RECORD (PROGRAM STEP 1). This LOW level signal is now applied to the DECODER boards to encode the character that has been selected from the jacks located on the MASTER BOARD. This character is now present on the LINE OUT outputs from the DECODER boards.

The momentary LOW from the gate at the input to the L.E. PROGRAM CODE flip-flop also set up a gate feeding the DATA and STROBE CLEAR REGISTER. This gate's output goes HIGH first and then LOW as its input goes HIGH. This triggers the DATA and STROBE CLEAR one-shot multivibrators. The "0" output of the DATA and CLEAR multivibrator goes LOW and activates gates to clear the STROBE GENERATOR flip-flop and activates gates to reset the OUTPUT DATA flip-flops. The "1" output of the DATA XFER ENABLE multivibrator goes HIGH for approximately 400 microseconds and then goes LOW. As the "1" output goes LOW the DATA XFER ENABLE one-shot is triggered.

The "1" output of this multivibrator goes HIGH, passes through two gates and activates one input of the DATA INPUT gates. Those gates with data on their second input (HIGH level signals) will now produce LOW level outputs. These LOW level signals are used to set their corresponding OUTPUT DATA flip-flops. The flip-flops that are set produce a HIGH level signal on their "1" output lead which is then inverted to a LOW level signal to correspond to a MARK condition.

When the "1" output of the DATA XFER ENABLE flip flop goes LOW, the DATA REGISTER CLEAR flip-flop is triggered and its "1" output goes LOW. This LOW level signal is applied to gates and becomes the LOW level DATA REGISTER (clear) signal. This signal will now clear the DATA REGISTERS (Location No. 3). The "0" output of the DATA REGISTER CLEAR flip-flop goes HIGH and is inverted to reset the L.E. PROGRAM CODE flip flop.

When the DATA XFER ENABLE flip-flop was triggered, its "0" output went LOW. After a period of 400 microseconds, this output again goes HIGH. This signal is inverted and used to trigger the STROBE GENERATOR flip-flop. The "0" output of this flip-flop goes HIGH. The HIGH level signal is fed to an inverter stage and becomes the LOW level STROBE signal transmitted to the receiving terminal as an indication that data may be read.

As the card procedes through the sensing area, both the T.E. and the L.E. phototransistors are covered producing HIGH level inputs on two of the three inputs to an AND gate. When a FORMAT MARK is recognized, the third input goes HIGH and a LOW output is produced. This LOW level signal produces GATED CLOCK (Window), sets the DATA REGISTER CLEAR flip-flop and activates the gate leading to the DATA and STROBE CLEAR flip-flop. This, of course, starts a new read sequence of clearing the OUTPUT DATA flip-flops and the STROBE GENERATOR flip-flop, enabling the DATA XFER ENABLE flip-flop, reading data and setting the OUTPUT DATA flip-flops and generating a strobe. This sequence will occur everytime a FORMAT MARK is recognized.

As the L.E. phototransistor is uncovered by the trailing edge of the document, an AND gate will produce a LOW output. When the T.E. phototransistor is uncovered by the trailing edge of the document, the AND gate output will again go HIGH. This signal (inverted) will trigger the T.E. PROGRAM CODE flip-flop and its "0" output will go HIGH. This HIGH signal is inverted and becomes the END of RECORD (PROGRAM STEP 2) signal. This LOW level signal is transmitted to the receiving terminal to indicate when a card has been read.

The EJECT flip-flop will recognize the EJECT code and enable the card to be transported through the reading area more rapidly, the same as for serial operation.

The LOGIC CLEAR gate clears the STROBE GENERATOR flip-flop and the OUTPUT Data flip-flops at the end of a card.

The PARITY GENERATION circuit determines whether or not a parity mark should be generated on the USASC II-85 Character and PTTC/BCD codes.

The circuit consists of dual input OR gates that receive their inputs from two different OUTPUT DATA flip-flops. The outputs of the OR gates are tied in groups of two. Each one of these groups in turn feeds other OR gates. (Two of these OR gates also receives one input apiece from the two outputs of one OUTPUT DATA flip-flop). The outputs of the second set of OR gates are tied in groups of two and again, each feeds a third set of OR gates. The third set of OR gates consists of just two gates. These in turn have their outputs tied together. Their output feeds an AND gate, either directly or through an inverter. The two different paths of feeding the AND gate allows for ODD or EVEN parity to be selected. The second input to the AND gate is the reset line for the OUTPUT DATA flip-flops, This line will always be at a HIGH level at this time. Regardless of whether the parity is ODD or EVEN, the cross connecting of the OR gates will cause a HIGH level signal to be produced at the input of the AND gate if a parity mark is needed. If a HIGH is received, the output of the AND gate will go LOW, indicating a MARK condition exists on the PARITY line.

H. DATA OUT BOARDS (Refer to Figures 70 to 74)

Data from the documents has now been recognized, decoded and encoded and processed by the TIMING and CONTROL LOGIC circuits. The output circuitry to supply the MODEM or Business Machine with the data is on the board in Location No. 8. There are three different boards which may be used in this location depending upon the device to which the data is transmitted.

1. Data Out-Phone (Refer to Figure 70)

The output of data from the TIMING and CONTROL LOGIC board (Serial Mode) is applied to the input of the DATA LINE DRIVER. This data is from an inverted OR gate circuit. Therefore, if a HIGH was placed in the SHIFT REGISTER, the output of the OR gate will be a LOW level signal and vice versa for a LOW. A LOW into the DATA LINE DRIVER will correspond to a "1" bit of information or a MARK. A HIGH at the DATA LINE DRIVER will correspond to a "0" bit of information or a SPACE. The bits on the line will be a MARK or a SPACE condition. The signals are applied to a data set or acoustic coupler.

With the input to transistor Q10 HIGH (4.5 Vdc to 5.0 Vdc) or SPACE, the collector becomes less positive, turning on transistor Q12. The collector of transistor Q12 becomes more positive. This places the output lines at +12 Vdc. Also, the base of transistor Q13 becomes less positive and the transistor will turn off.

If the input to transistor Q10 is LOW (0.0 Vdc to 0.5 Vdc) or a MARK, Q10 will be cut off, making the base of transistor Q12 positive and cutting it off. The collector of Q12 now swings negative, placing the base of Q11 less positive and cutting Q11 off. This allows the base of transistor Q13 to become less positive, turning on Q13. As a result, the output line becomes a -12 Vdc. The output transistors Q12 and Q13 are a complimentary pair and the output is from +12 Vdc for a SPACE to -12 Vdc for a MARK condition.

On the board in Location No. 8 is the PHONE LINE VALIDITY CHECK circuit. One of the last "handshaking" signals between the MDR and its interface is the receipt of CB·SB (or CB·CF) by the Document Reader. That signal is received by the PHONE LINE VALIDITY CHECK circuit. Upon receiving the signals (HIGH level signals), transistors Q1 and Q2 turn on, which turns on transistor Q3. Transistor Q3 then forward biases transistor Q4 and it turns on. When Q4 turns on, transistor Q5 is reversed biased and cut off. This allows capacitor C1 to charge and after a time delay (determined by the setting of Potentiometer R11) transistor Q6 is turned on. When Q6 is turned on, transistors Q7 and Q8 will be turned on. The collector voltage of Q8 will go LOW and be applied to two inverters. One inverter will apply a HIGH level input to transistor Q9, turning it on. This applies a ground to the SEND light on the OPERATOR'S PANEL, and the light will turn on. This indicates that data may now be sent. The second inverter feeds a HIGH level signal to the FEED LOGIC board (Location No. 9) as an internal CB·SB signal. This signal will initiate a CARD FEED.

The delay circuit (variable from 1 to 12 seconds) is to allow for any noise on the line, produced by connecting, to dissipate before sending any signals. If the delay need not be used, a jumper will allow the delay circuit to be bypassed.

A third circuit contained on this board is the POWER ON PRE-CLEAR. When power is first applied, both transistors (Q14 and Q15) are turned on which applies a LOW level signal to the TIMING and CONTROL LOGIC board. This LOW level signal is used to clear several flip-flops on the TIMING and CONTROL LOGIC board. After a short period of time, capacitor C2 charges to a potential such that Q14 and Q15 turn off. The circuit will have no further effect on the MDR operation until the next time that the unit has power applied.

The DATA OUT-PHONE board also contains the BIT OSCILLATOR circuit (Refer to Figure 71). The BIT OSCILLATOR board plugs into the DATA OUT-PHONE board. In order to interface with different modems, two BIT OSCILLATOR frequency rates are used. These are 110 Hz and 1050 Hz. Capacitors C1 through C6 are changed to achieve the two operating frequencies. Fine adjustment of frequency repetition rates is accomplished by adjusting potentiometer R3.

The BIT OSCILLATOR is a free-running multivibrator circuit. As such, it will be generating a continuous square wave. The collector of the output transistor Q2 is alternately going first HIGH and then LOW. With every transition from LOW to HIGH, an output from the INVERTER will be produced that is a HIGH to LOW signal. This signal is applied to the TIMING and CONTROL LOGIC board. When the TRIGGER ENABLE circuit is activated, the BIT OSCILLATOR output is now allowed to perform its timing function.

2. Data Out - TTY (Refer to Figure 72)

When the MDR output is to a teletypewriter, a different output circuit is required. The output circuitry is a TELETYPE RELAY DRIVER circuit. When power is first applied, transistors Q7 and Q8 both turn on and clamp Q9 off. With Q9 off, Q1 will be non-conductive and the output from the DRIVER will be HIGH or +12 Vdc. This places a MARK on the SERIAL DATA OUT line. Then, when data is being received by the DRIVER circuit, a SPACE input will turn on Q1 placing a ground or LOW on the SERIAL DATA line. This corresponds to a SPACE condition on the line. A MARK input to the DRIVER turns off Q1 placing +12 Vdc or a MARK condition on the SERIAL DATA line. The SERIAL DATA line is connected to the teletypewriter adapter.

The teletypewriter adapter (refer to Figure 73) contains a relay whose contacts are normally closed. This keeps a closed loop on the output and allows line current (60 mA or 20 mA) to flow in the circuit. As was mentioned above, when the unit was turned on, the SERIAL DATA line was held HIGH (+12 Vdc). Relay K1 will not energize and the current loop is not broken. Under a SPACE condition, relay K1 receives a ground from the SERIAL DATA LINE. The relay energizes and the contacts open, breaking the current loop. This represents a SPACE condition to the teletypewriter. Then when the

SERIAL DATA LINE is in the MARK condition again (HIGH) the relay will not be energized and the contacts will be closed, allowing loop current to flow. As the DATA line changes from SPACE to MARK and back again, the current on the line will go from SPACE (no current) to MARK (60 mA of current) and back again.

The teletypewriter adapter also contains a sensing circuit. When current is flowing in the loop, a signal is coupled through transformer T1 to the base of transistor Q1. This signal turns on Q1 causing its collector to produce a negative pulse. This pulse will be applied to the DATA OUT - TTY board to indicate when information is being sent on the line.

The TELETYPE BUSY LIGHT INDICATOR CIRCUIT (refer to Figure 72) receives the pulse from the sensing circuit in the teletype adaptor. This pulse triggers a monostable multivibrator. Transistor Q4 is triggered off and transistor Q5 is turned on as a result. When Q5 turns on, transistor Q6 is biased off and turns off the

SEND indicator light. When the monostable relaxes to its quiescent state, Q6 again turns on and the SEND indicator lights again. Every time a pulse (indicating information on the line) is received, the light will go out momentarily. Thus, the flashing light informs the observer that information is on the line and the line is busy.

A POWER ON PRE-CLEAR circuit, identical to the circuit on Figure 70 is used again to clear flip-flops as the unit is turned on. After the unit is on, the circuit has no other function.

3. Interface Driver (Parallel) (Refer to Figure 74)

When information is presented in parallel form, all bits must be supplied to the Business Machine at one time. Therefore, each LINE OUT from the TIMING and CONTROL LOGIC board has its own DATA LINE DRIVER circuit. This includes all 12 data rows, the STROBE output, the END OF CARD output and, from their sense amplifiers, the L. E. and T. E. signals. All these DATA LINE DRIVERS are identical.

The inputs from the DATA ROWS to the DATA LINE DRIVERS will be a HIGH level for a SPACE and a LOW level for a MARK condition. Upon receipt of a SPACE (HIGH) the DATA LINE DRIVER transistor turns on and its output goes LOW. This LOW level signal will be supplied to the Business Machine as a SPACE condition. If the input to the DATA LINE DRIVER is a MARK (LOW) condition, the transistor will turn off and provide a HIGH level condition for a MARK to the Business Machine. The HIGH level output will be either +12 Vdc or +5 Vdc depending on the requirements of the Business Machine. This is accomplished by placement of a jumper on the board.

The input from the STROBE signal will be identical to the signal from the DATA ROWS. However, the signal from the END OF CARD is the reverse. An INVERTER stage reverses the END OF CARD signal to produce the same input to its DATA LINE DRIVER as the DATA ROWS and STROBE to theirs.

The L. E. and T. E. signals, which tells the Business Machine that a card has entered and then left the sensing area, are applied through inverters to an OR gate. The output of the OR gate is inverted and applied to a DATA DRIVER stage to produce a HIGH level output as long as the card is in the sensing area. Since the L. E. and T. E. signals are applied to an OR gate, the output signal exists from the time the L. E. phototransistor is covered by the leading edge of the card until the T. E. phototransistor is uncovered by the trailing edge of the card.

Two signals from the Business Machine are received on this board and then applied to circuits on the TIMING and CONTROL LOGIC board. These are DATA RESET and STROBE RESET. Both are LOW level signals. When they are received, diode CR1 (CR2) is forward biased which reverse biases CR3 (CR4). As a result, transistor Q16 (Q17) is cut off. Its output goes HIGH and is inverted to a LOW level signal. The LOW level signals are applied to OR gates on the TIMING and CONTROL LOGIC board, one to reset the STROBE GENERATOR flip-flop and one to reset the OUTPUT DATA flip-flops.

Also contained on the board is a POWER ON PRE-CLEAR circuit to insure that flip-flops on the TIMING and CONTROL LOGIC board are cleared when the unit is turned on.

I. FEED LOGIC (Refer to Figure 75)

The CARD FEED LOGIC board (Location No. 9) is used to activate the CARD FEED SOLENOID after the circuitry ascertains that the motor is up to speed and that all needed signals are present.

Upon receipt of the "handshaking" signal CC, the MOTOR ENABLE circuit is activated. Transistor Q1 is cut off by the CC signal. This allows capacitor C1 to charge which triggers transistor Q2 after a 1.2 second delay. This delay allows time for the motor to get up to speed before a card feed may occur.

When transistor Q2 turns on, transistor Q3 is forward biased and when Q3 turns on, a forward bias is applied to transistor Q4. Transistor Q4 now conducts and as its collector goes LOW, the output is inverted and applied as a HIGH level signal to one input to an AND gate. The other input is CB·SB, an internal signal created upon receipt of CB·SB from the Modem, from the DATA OUT-PHONE board (Location No. 8).

The AND gate now produces an inverted (LOW) output which, in turn, is inverted to a HIGH and applied to one input of a second AND gate. A second input is derived from the T. E. sense amplifier. With no card in the sensing area, the input to the FEED LOGIC board is LOW but this is inverted to a HIGH at the input to the AND gate. Now the unit is ready to start feeding cards.

When the CARD FEED switch on the OPERATOR'S PANEL is depressed, a LOW level signal is applied to the base of transistor Q5 and the transistor is cut off. Its output now goes HIGH and then becomes a LOW level signal through an inverter. This LOW level signal is tied to an input to the AND gate but is also tied to the SET input to the ONE CARD INHIBITOR flip-flop. The "1" output of the flip-flop goes HIGH and this HIGH is applied back to the third input of the AND gate. Now when the FEED switch is released, transistor Q5 turns on again and its output goes LOW. This output is inverted and is applied to the AND gate. This is the third HIGH input and a LOW is produced in the output of the gate. Transistor Q6 now turns off, allowing capacitor C3 to charge. After 60 ms, the unijunction transistor will turn on. A positive pulse is coupled from T1 to the input to a gate which produces a LOW level output. This signal is applied to an OR gate whose output now goes HIGH. When the positive pulse out of T1 ends, the OR gate output goes LOW. This now triggers the one-shot multivibrator. The "1" output becomes HIGH and is applied to an AND gate. The other input is already HIGH (from CB·SB) and the

gate produces a LOW. This LOW, inverted through a gate to a HIGH, turns on Q7. This provides a ground to the CARD FEED SOLENOID and a card feed is initiated.

The "0" output of the one-shot goes LOW when the multivibrator is triggered. This LOW resets the ONE CARD INHIBITOR flip-flop. This, in turn, removes a HIGH from one input of the AND gate on the input of the Unijunction Oscillator. Transistor Q6 now conducts and the oscillator is now shut down.

As the end of a card leaves the sensing area, a card feed trigger from the TIMING and CONTROL LOGIC board enters the FEED LOGIC board and initiates another card feed. This action will continue until the last card has been fed.

J. ALARM LOGIC (Refer to Figures 76, 77 and 78)

Alarm circuits used for signaling and indication purposes are located on the boards in Location No. 10. There are three boards that may be used, the ALARM -BEL and the HOPPER EMPTY for the serial mode of operation and the READER CONTROL INTERFACE for the parallel mode of operation. If no alarm options are used, the slot in the card cage for Board No. 10 is left empty.

1. Alarm-Bel (Refer to Figure 76)

This board used on automatic unattended units contains two options. The first circuit (Alarm Option) gives an audible alarm whenever a card has not been fed for 12 seconds. The circuit receives the internal CB*SB which places a HIGH on one input of an AND gate. The other input is from GATED CLOCK (Logic). This input goes LOW every time a FORMAT MARK is recognized. If this input stays HIGH (no card being fed), the AND gate produces a LOW output which turns off transistor Q1. Capacitor C1 is now allowed to charge and after 12 seconds, transistor Q3 turns on. Transistor Q5 now becomes forward biased. As Q5 conducts, transistor Q6 receives a forward bias and conducts. Transistor Q7 now is turned on by a positive going voltage on its base. The collector of Q7 is now LOW and a ground is placed on the audible alarm turning it on. A red ALARM light on the Operator's Panel also lights. The alarm can be disabled by a switch on the back of the Document Reader.

The second circuit is the HOPPER EMPTY option. This circuit recognizes when the last card has left the hopper and has been read. It then sends a signal to the BEL flip-flop on the TIMING and CONTROL LOGIC board. The output of the T. E. sense amplifier is applied to a gate and an inverted output is produced. At the end of the last card, this output goes HIGH. This HIGH is applied to one input of an AND gate. A second input is from the internal CB*SB signal which is HIGH. The third input is from the R-S flip-flop. As all inputs are now HIGH, the output of the AND gate goes LOW. This signal now cuts off transistor Q2.

When the last card leaves the hopper, the normally open contacts of the ALARM and BEL actuate switch close and apply +12 Vdc to the circuit. Capacitor C2 charges and after 1.2 seconds, transistor Q4 turns on. The transistor conducts and a positive pulse is coupled out of transformer T1 to a gate. The LOW output of the gate is applied to the BEL flip-flop on the TIMING and CONTROL LOGIC board and a BEL code is transmitted.

An output from the gate also sets the R-S flip-flop which, in turn, disables the three input AND gate. Transistor Q2 turns on, discharges C2 and transistor Q4 turns off. Thus only one BEL signal is sent.

2. Hopper Empty (Refer to Figure 77)

This circuit used on automatic attended units provides for an audible alarm when the last card has left the hopper. At that time, the normally open contacts of the HOPPER EMPTY switch close, placing a positive voltage on the base of transistor Q1. The transistor conducts and a ground is supplied to the alarm, turning it on. A red ALARM light on the Operator's Panel also lights. The audible alarm may be disabled by a switch on the back of the Document Reader.

3. Reader Control Interface (Refer to Figure 78)

The READER CONTROL INTERFACE board contains three different circuits. One circuit is used for alarm purposes while the other two are performing control functions on signals received from the interface equipment.

(a.) Alarm Contról Circuit

The ALARM CONTROL circuit receives an input from the HOPPER EMPTY switch. After the last card has left the hopper, a +12 Vdc is applied to the base of transistor Q1. This transistor will turn on, placing its collector at ground potential. The ground will be applied to the audible alarm turning it on. This alerts the operator that the hopper is empty and either more cards must be inserted or the MDR is to be disconnected from the interface equipment.

(b.) Motor Enable Circuit

The MOTOR ENABLE circuit receives its input from the interface equipment. When data is desired from the MDR, the input signal will go HIGH. This reverse biases CR2 and forward biases CR3. Transistor Q2 will now conduct and its collector will become LOW. This LOW level signal is applied to three inverter stages. The first inverter feeds a second inverter. The output of this second inverter goes LOW and is applied as a CC (Data Set Ready) signal to the FEED LOGIC board (Location No. 9). This allows the sequence to start that will permit a card feed to be initiated.

The second inverter on the output of transistor Q2 supplies a HIGH level signal to

the base of transistor Q3. This transistor will now conduct and its collector circuit will supply a ground to the motor relay (K3). Relay K3 will energize and the motor of the Document Reader will start.

When all data has been read, the interface device will cause the MOTOR CONTROL input to go LOW which will remove the CC signal and drop out Relay K3.

The third inverter on the output of transistor Q2 is feeding one input of an AND gate in the CARD FEED CONTROL circuit.

(c.) Card Feed Control Circuit

When a CARD FEED is to be initiated, the interface equipment will supply a CARD FEED CONTROL input signal which will be a HIGH level signal. This HIGH will reverse bias CR6, allowing CR7 to be forward biased. Transistor Q4 will now conduct and its collector will go LOW. This LOW is inverted to a HIGH and applied to the FEED LOGIC board (Location No. 9) to initiate a card feed. The output of the inverter (HIGH) is also applied to an input of an AND gate. The other input is a HIGH supplied through an inverter from the output of transistor Q2 in the MOTOR ENABLE circuit. The output of the AND gate goes LOW and then through another gate becomes a HIGH signal. This turns on transistor Q5, applying a ground to the SEND light on the operator's panel. This serves as an indication that data may be transferred.

After the last card in the hopper has been read, another CARD FEED CONTROL signal will be required from the interface equipment in order to read more cards.

K. INTERFACE CONTROL BOARDS (Refer to Figures 79 and 80)

There are two different boards that may be used in Location No. 11. These two are used for different modes of serial operation. The functions that are performed on these boards are the "handshaking" routines between the Document Reader and the interface device. The recognizing and generation of these signals must be accomplished before communications between the Motorola Document Reader and the interface device may be established.

1. Phone Control-Unattended (refer to Figure 79)

When power is applied through the switch on the operators panel, a relay (K1) in the power supply is activated and latched. Power will now be supplied to the power supply. At this time, transistor Q9 will turn on which will forward bias transistor Q10. As Q10 turns on, its collector will go HIGH and CD (Data Terminal Ready) will be sent to the interface device.

When CD is received by the interface device, CC (Data Set Ready) will be immediately returned to the MDR. (In some cases, the signal to be returned will be CF (Data Carrier Detector). Either CC or CF may be used.) When CC (or CF) is received by the Document Reader (a HIGH level signal), transistor Q1 will turn on which turns on transistor Q3 which in turn will cause transistor Q4 to turn on. The collector of transistor Q4 now goes LOW. This LOW level signal is applied to two inverters. The output of one inverter (a HIGH level signal) turns on transistor Q5 which supplies a ground to the Motor Relay K2. The MDR motor will now start.

NOTE

If CD does not go HIGH when the unit is turned on, the PHONE DISCONNECT DELAY CONTROL circuit will activate and cause CD to go HIGH after 40 seconds delay.

The HIGH level output from the second inverter is applied through two more inverters to transistor Q8 which turns on. This applies forward bias to transistor Q11. When transistor Q11 turns on, its collector goes HIGH. This is the CA (Request to Send) signal which is sent to the interface device. Upon receipt of CA, the interface device will return CB·SB and communications between the MDR and the interface device is established. The signal CA may also be initiated by pressing the FEED switch on the operator's panel. This produces a MANUAL CA signal from the FEED LOGIC board (Location No. 9) which is applied to the inverter prior to transistor Q8.

A third output from transistor Q4 is to one input of an OR gate. The output of the OR gate (HIGH) is applied to one input of an AND gate leading to the PHONE DISCONNECT DELAY CONTROL circuit. The second input to the AND gate is GATED CLOCK (Logic). This signal is normally HIGH which produces a LOW output from the AND gate. This will turn off transistor Q6, allowing capacitor C1 to charge and fire the unijunction transistor Q7. When transistor Q7 turns on, a positive pulse of 40 seconds duration is developed in the output of transformer T1. The trailing edge of this pulse will trigger the J-K flip-flop, producing a HIGH output on its "1" output. The result of this is that the CD signal will go LOW, disconnecting the interface device from the MDR. With the CD signal removed, CC (or CF) will also be removed which would remove the LOW input to the OR gate on the output of transistor Q4 and turns the Document Reader off by dropping Relays K2 and K3. However, the "0" output of the J-K flip-flop is LOW, keeping the output of the OR gate HIGH. This allows the unijunction transistor Q7 to produce another 40 second positive pulse. On the second pulse's trailing edge, the J-K flip-flop is again triggered. The "1" output now goes LOW, reestablishing CD out and the "0" output goes HIGH, causing the output of the OR gate to go LOW. The AND gate leading to the PHONE DISCONNECT DELAY CONTROL circuit now produces a HIGH which turns on transistor Q6. This places a shunt across capacitor C1 which shuts down the unijunction transistor Q7 and no more pulses will be produced.

The above mentioned sequence will only occur if communications between the MDR and the interface device had been established and no cards were being fed. If cards were being read, GATED CLOCK (Logic) would go LOW every time a FORMAT MARK was recognized. This would allow transistor Q6 to turn on momentarily, discharging capacitor C1 and thus preventing unijunction transistor Q7 from turning on.

A final circuit on this board is the RELAY DRIVER Circuit. When CB·SB is received from the interface device (upon receipt of CA from the MDR) a POWER INITIATE OFF signal was generated on the FEED LOGIC board (Location No. 9). This signal is applied to the RELAY DRIVER circuit which applies ground to Relay K3. When Relay K3 is pulled in, it will cause Relay K1 to be de-energized. Now when the "handshaking" signals are removed, the relays (K2 and K3) are automatically dropped out, shutting down the Document Reader until communication is established once again.

2. Phone Control - Attended (Refer to Figure 80)

When the Motorola Document Reader is to be in the attended operation mode, the automatic signal recognizing and shut down features are not needed. Therefore, all that is required is to produce the two "handshaking" signals that must be sent from the Motorola Document Reader to the interface device. This is accomplished by connecting two resistors to +12 VDC. The other ends of the resistors are the two signals required, CD (Data Terminal Ready) and CA (Request to Send). These signals will always be present as long as the unit has power applied and will cause the interface device to return CC (or CF) and CB·SB to the Document Reader.

L. POWER SUPPLY (Refer to Figure 81)

When power is first supplied to the unit, Relay K1 is energized, supplying power to transformers T1 and T2. This in turn provides power to the three separate sections of the power supply. Once the supplies are operating, voltage is available (+15 Vdc) to energize Relays K2 and K3. On automatic unattended units, when Relay K3 is energized, it will cause Relay K1 to de-energize. This permits automatic shut down of the MDR by removing the signals that caused K2 and K3 to be energized. On attended units, a jumper plug in the K2 socket is used and the unit needs no signals to turn it on once power is applied.

1. Lamp Power Supply

The secondary of transformer T1 supplies a-c voltage to the bridge rectifier CR1. The rectified voltage is filtered and applied to the regulator circuit. Series regulator transistor Q1 (2N1544) has its base potential controlled by the conduction of transistor Q2. Transistor Q2 has its base voltage controlled by a Zener diode regulated voltage divider network. Potentiameter R4 permits adjustment of the lamp voltage to obtain proper brilliance.

Transistors Q3 and Q4 supply the current to light the READY indicator on the operator's panel. The base circuits of transistors Q3 and Q4 are the positive lamp supply. As long as all the Sensor lamps are lighted, the transistors will conduct and the READY indicator will light. If a Sensor bulb burns out, transistor Q3 or Q4 will be biased to cut off and the READY indicator will go out. Transistor Q1 on the printed circuit board controls the amount of voltage applied to the READY indicator. The lamp voltage is normally 17.0 volts $\pm$ 1.0 volts.

2. IC Power Supply

One secondary of transformer T2 supplies voltage to bridge rectifier CR1. A regulator circuit consisting of transistors Q1, Q2 and Q3 and external transistor Q2 (2N3715) are used to provide regulation for the voltage supplied to the integrated circuits. Potentiameter R7 provides for exact adjustment of the +5 Vdc out of the power supply. Transistor Q2 on the board controls the base potential and thus the conduction of the series regulator transistor. Transistors Q1 and Q3 balance the base potential of Q2 between them, thereby controlling its conduction. This provides a fine degree of control.

Transistor Q4 is across the output of the supply to sense if the output voltage rises too high. If this were to happen, transistor Q4 would turn on, feeding a positive voltage to the gate of SCR1, turning it on. This would place a heavy load across the bridge rectifier and cause the fuse F2 to blow. The integrated circuits are thus protected from excessive voltage.

3. Component Power Supply

The component power supply need not be as heavily regulated and thus has only a two stage regulator circuit. Also, no adjustment of the output voltage is available. The output voltage should be +12.0 Vdc +15 Vdc. This +12 Vdc combined with a -12 Vdc output from the Lamp Power supply is used for the output voltages for the DATA LINE DRIVER stages. The +12 Vdc also powers other discrete component stages.

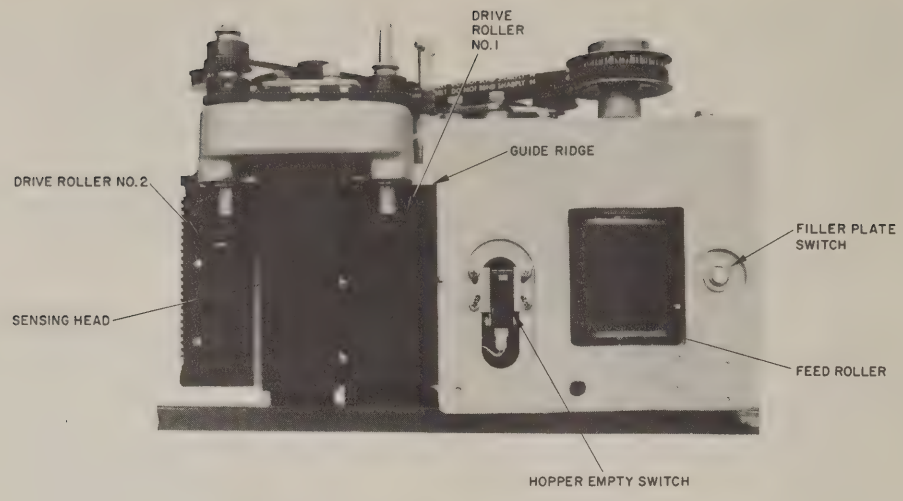
A circuit consisting of Zener diode VR2 and resistor R4 senses if the output voltage is exceeding the maximum allowable potential. If the voltage becomes excessive, the diode conducts, placing a positive potential on the gate of SCR1. This will place a heavy load across the bridge rectifier CR1 and cause fuse F3 to blow.

A +15 Vdc output is available as a potential to energize relays.

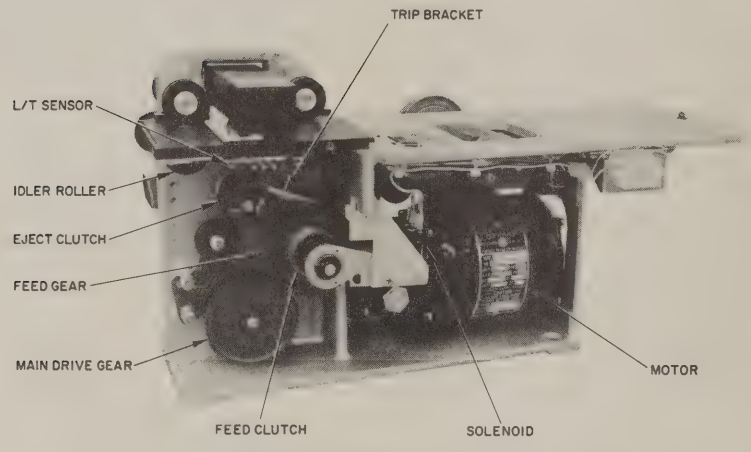
M. CARD TRANSPORT THEORY OF OPERATION

The basic transport mechanism positions, and controls the speed of the document as it passes through the sensing area. When the MDR is equipped to automatically feed cards, three additional functions are provided by the transport mechanism. These are to store, feed, and eject cards.

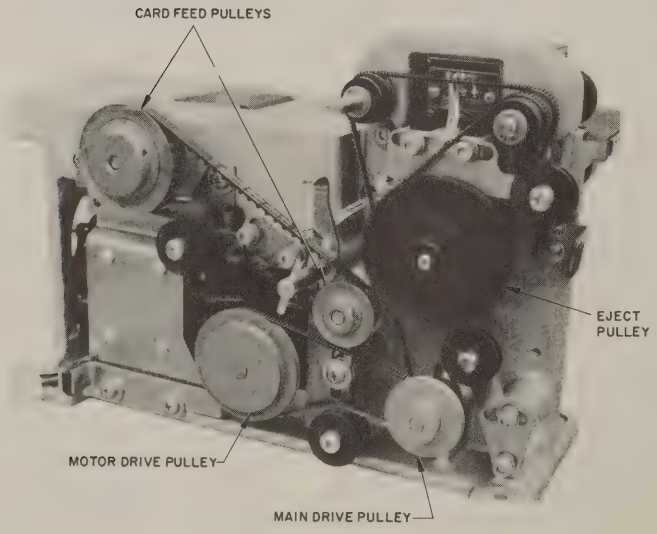
Figure 31 shows three views of an automatic transport mechanism.



(a) Top View



(b) Left Front View



(c) Right Rear View

Figure 31. Automatic Feed Transport Mechanism

1. Basic Operation (Refer to Figure 31)

The basic transport mechanism operates in the following manner:

With 117 Vac applied to the motor, the motor drive pulley runs at a constant speed while driving the main drive pulley. The main drive pulley drives the drive rollers which, in turn, drive their associated idler rollers.

When a document is manually fed into the unit, drive roller No. 1 and its associated idler roller grasp the document and advance it toward the sensing head. At the same time, they position the edge of the document flush against the guide ridge.

As the document passes through the sensing area, its leading edge enables the leading and trailing edge phototransistors on L/T sensor board. This event prepares the MDR for data. The document continues to be pushed through the sensing area until it comes into contact with drive roller No. 2.

Drive roller No. 2 also holds the document against the guide ridge while it pulls the document through the sensing area. As the document passes through the sensing area, the 13 phototransistors detect the data contained on the document and transfer the data to the amplifiers.

The end of the document disables the leading and trailing edge phototransistors as it leaves the sensing area. This event allows the MDR to prepare for another document. Driver roller No. 2 continues to pull the document through until it leaves the transport mechanism.

The transport can accept another document any time after the end of the document has cleared the sensing area.

2. Automatic Operation (Refer to Figure 31)

When automatically feeding cards, the transport mechanism operates in the following manner:

The motor drives the motor drive pulley at a constant speed. The main drive pulley is driven by the motor drive pulley. It drives the main drive gear and the driver rollers through its shaft. The drive rollers, in turn, drive their associated idler rollers while the main drive gear drives the feed gear. The feed gear tries to drive the feed clutch which is disabled by the solenoid. The main drive shaft also tries to drive the eject clutch which is disabled by the trip bracket.

When a card is to be fed, the solenoid momentarily energizes and releases the feed clutch. The feed clutch grasps the feed shaft and causes it to rotate. This rotation, in turn, causes the card feed pulleys to turn. The card feed pulleys then rotate the feed roller which forces the bottom card in the hopper through the hopper feed gate. The feed roller continues forward until the feed clutch is again disabled by the solenoid stop. By this time, the card has already entered drive roller No. 1 and is being pushed through the sensing area. The travel of the card through the sensing is identical as stated in the basic operation.

At the same time that the solenoid releases the feed clutch, a cam on the feed shaft raises the trip bracket. This allows the eject clutch to enable and grasp its shaft. The eject shaft drives the eject pully which increases the speed of drive roller No. 2. Drive roller No. 2 now rotates six times faster than drive roller No. 1.

When the first card is fed through the transport, the eject operation performs no useful function. Thereafter, each card is ejected at six times its normal speed after its trailing edge clears the trailing edge phototransistor or a "Card Eject" code has been detected on the card after column 12 on a 40-column card or column 24 on an 80-column card.

VII. SERVICING AND REPAIR INFORMATION

A. RECOMMENDED TEST EQUIPMENT

The following test equipment is recommended for the repair and servicing of the MDR Document Reader.

Test Equipment	Part Number
• Test Set	01-F7711G01
• Service Feet	75-F7792G01
• Volt/Ohm Meter	S1052B
• 44-Pin Extender Card	84-F7790G01
• 70-Pin Extender Card	84-F7791G01
• Oscilloscope	S1301A or equivalent
• IBM Tab Card Registration Gauge	450770 (IBM part number)

The following hand tools should be available when servicing the MDR:

- screwdrivers - phillips, flat blade
- wrenches - allen (1/4" and smaller), ignition set (7/16" and smaller)
- pliers - needlenose, sidecut, duckbill, truarc
- soldering iron (40W), soldering aid, scribe, solder sucker (Edsyn, Inc. - Soldapullit), solder
- punches - center (1/4" tapered tip), brass flat (1/4" tapered tip)
- wire stripper, crimper, electrical tape
- small magnet, small magnifying glass, 6" steel ruler, X-acto knife
- tweezers, hemostats, jeweler's files, feeler gauges (.001 - .025)
- rubber mallet, toothbrush
- push-pull pound scale (Chatillon No. 767)

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B. INSTALLATION PROCEDURES

1. Unpacking and Handling

The MDR Document Reader is shipped in a specially constructed carton which provides protection from normal shock and vibration. However, abusive handling should be avoided.

To remove the Document Reader, set the carton in an upright position. Open the top of the carton and dismantle one side of the carton.

Remove the accessory carton and then remove the Document Reader by lifting the wooden platform out of the carton.

Remove the three shipping bolts from the underside of the wooden platform.

CAUTION

Do not allow the Document Reader to fall off the platform.

The Document Reader and its accessories should be inspected for any damage incurred during shipment. All equipment is carefully inspected and free from defects before it is packaged for shipment at the factory.

Verify the model number of the Document Reader agrees with the model number that was ordered.

2. Setup

Refer to MDR Operator's Manual. Perform the Initial Setup procedure for the type of operation normally used.

3. Interface Connections

Generally, there are three main types of interface devices which operate with the MDR Document Reader. These are: teletypewriter sets, acoustic couplers, and data sets.

To connect the interface device to the Document Reader:

- For Teletypewriter Sets, connect the two current leads to the TTY Adapter screw-on terminals on rear of Document Reader.
- For Acoustic Couplers, connect the 9-foot cable from output connector J15 on the Document Reader to the acoustic coupler.
- For Data Sets, connect the 9-foot cable from output connector J15 on Document Reader to the data set.

C. DOCUMENT READER OPERATIONAL CHECK-OUT

1. Plug power cord into 114 Vac, 60 Hz receptacle.
2. Press POWER switch to ON potition.
3. Verify the READY indicator lights. If not, proceed as follows.

   (a.) Check blower. If blower is not operating:

   (1) Check Fuse F1.

   (2) Check output from power receptacle.

   (3) Check power supply using Figure 81.

   (b.) Check lamp board. Verify all lamps illuminate. (Extender board 01-F7709G01 - part of Test Set - should be used.)

   (1) If one or more lamps are not illuminated, replace lamp board with spare lamp board.

   (2) If all lamps are out, refer to Figure 55.

   - Check lamp supply fuse.
   - Check transistors Q3 and Q4 in lamp supply.

4. Connect Document Reader to MDR Test Set.. Refer to Instruction Manual for MDR Test Set, Model TE1.
5. Using the MDR Test Set, verify the Document Reader operates correctly. Refer to Instruction Manual for MDR Test Set, paragraph D, Test Procedure.
6. Disconnect MDR Test Set and restore Document Reader to normal operating condition.

D. GENERAL PREVENTATIVE MAINTENANCE

1. Cleaning and Lubricating

The MDR Document Reader is an office-type machine that requires limited maintenance with proper handling. The Document Reader should be inspected periodically for excessive dirt and cleaned when deemed necessary.

Isopropyl alcohol or Freon TE applied to a lint-free cloth should be used for cleaning agents.

Particular attention should be given to the following areas:

Part	Location	Procedure
Hopper Card Gate	Fig. 43, Item 7	Inspect for accumulated dust, excessive wear, and burrs.
Power Supply	Fig. 43, Item 75	Inspect for dust.
Operator Panel	Fig. 43	Inspect for cleanliness, switch operation and damaged lamp covers.
Idler Rollers	Fig. 44, Item 43	Inspect for cracked, or broken rollers, excessive dirt build-up.
Drive Frame	Fig. 44, Item 89	Inspect card area for dirt and chaff.

Part	Location	Procedure
Feed Roller	Fig. 44, Item 8	Inspect for dirt build-up within ribs on roller. Rotate feed mechanism to check entire roller.
Anti-Static Bracket	Fig. 44, Item 71	Inspect bracket for excessive wear.
Card Receiver Latch	Fig. 44, Item 72	Inspect for security.
Hopper Empty Switch	Fig. 44, Item 46	Verify switch operates, (Audible sound when pressed.)
Filler Plate Switch	Fig. 44, Item 53	Verify switch operates, (Audible sound when pressed.)
Bearing		Check for oil leakage. Wipe clean.
Belts		Inspect for wear and proper tension.
Sensor Lamp Assembly	Fig. 45, Item 1	Remove and wipe clean.
Motor	Fig. 45, Item 38	Inspect for oil leakage.
Drive Rollers	Fig. 45, Item 10	Inspect for excessive wear, end-play, and dirt build-up.
Hold Down Spring	Fig. 45, Item 29	Inspect for excessive wear and proper positioning.
Hopper	Fig. 43, Item 5	Insure proper fit when installed.
Hopper Empty Button	Fig. 43, Item 9	Inspect for freedom of movement and, when depressed, for operation of Hopper Empty switch.
Filler Plate	Fig. 43, Item 4	Insure proper fit when installed. Check moveable card guide for proper operation.
Card Receiver	Fig. 43, Item 1	Verify deflector operates smoothly. Check for proper positioning when installed.

The design of the Document Reader (sealed bearings, life-time blower and motor, plastic gears and pulleys) eliminates the need of applying lubricants.

2. Mechanical Checks

With the hopper completely filled with cards and the card weight in place, cards should be fed smoothly and transported through the read station at an even rate of speed. The top of the card should be positioned squarely against the edge of the drive frame guide ridge.

The card should have a snappy eject, and immediately clear the read station when the next card is being fed or an "eject" code is marked on the card being read.

Cards should not bind nor faulter during feeding nor should cards bind or stack incorrectly in the card receiver so as to interfere with other cards..

3. Electrical Checks

Data sensitivity should be adjusted to read test cards that have a 20% or more ink density. The Motorola Test Card #7225-29 can be used. Data should be detected beginning at column 14 and continue for the remainder of the card. If only a portion of the data is detected, then the sensitivity needs to be increased. Adjust the SENSITIVITY potentiometer A1A1R73 counterclockwise in 1/4-turn increments. (Access to the potentiometer is available through the hole in the top of the drive frame.)

If data is detected before column 14, the sensitivity is too high. Adjust the SENSITIVITY potentiometer A1A1R73 clockwise in 1/4-turn increments.

If data is intermittent when machine seems to be reading in the 20% area of the test cards, the format clock sensitivity may be too low. Adjust the potentiometer closest to the connectors in Location No. 2. Adjust potentiometer until all format marks are detectable; 1/4 turns counterclockwise to increase sensitivity and 1/4 turns clockwise to decrease sensitivity.

If the leading edge is being missed (usually programmed to give a carriage return), the LE potentiometer A1A2R9 (potentiometer farthest from connector pins on circuit board in Location No. 2) should be adjusted. The LE potentiometer A1A2R9 should be adjusted in increments or decrements of a 1/4 turn; counterclockwise will increase sensitivity, and clockwise will decrease sensitivity.

If the trailing edge is being missed (usually programmed to give a rubout), the TE potentiometer A1A2R15 (center potentiometer on circuit board in Location No. 2) should be adjusted. The TE potentiometer A1A2R15 should be adjusted in increments or decrements of a 1/4 turn; counterclockwise will increase sensitivity, and clockwise will decrease sensitivity.

NOTE

When making all sensitivity adjustments, it is very important to remember not to over adjust. A circuit that is over sensitive can give as many errors as one that is not sensitive enough. Always use clean test cards to determine if the sensitivity needs to be adjusted..

E. TROUBLESHOOTING PROCEDURE

The primary starting point for any problem is to obtain all the pertinent information relating to the problem and

to analysis this information. In many cases, vague or misleading information will be relayed to the serviceman. A helpful procedure to follow is:

- find the person who actually experienced the problem.
- listen to his description of the problem.
- have him amplify on areas of misunderstanding.
- familiarize yourself with the customer's operation
- perform the operation that initiated the service call

In general, a casual conversation can do more to establish and clarify what has happened as opposed to what was reported to have happened. All problems can be classified into two categories:

- those that are caused by the operator or by the associated equipment (documents or modems) and appear to be MDR problems
- those that are caused by the MDR

By determining the circumstances, most problems can be easily classified as to their cause. Others will require operating and testing of the units involved before they can be classified. A working knowledge of the basic operation of the system will enable you to locate most problems in a short time. Table 8 lists some of the most common types of problems and possible causes.

F. MECHANICAL AND ELECTRICAL ADJUSTMENTS

1. Mechanical Adjustments

CAUTION

Before proceeding with any mechanical adjustment, turn power off, unplug ac power cord, and disconnect any external connection to output cable connector J15.

a. Motor (38, Fig. 45)

(1) Perform Steps G11. a and b.

(2) Loosen motor mounting plate screws (41, Fig. 45).

(3) Position motor on its mounting pads.

NOTE

The motor should not touch any part of the frame or the power supply.

(4) Tighten motor mounting plate screws.

NOTE

A slight additional adjustment may be possible by loosening the motor mounting screws (37, Fig. 45).

PROBLEM	MOTOROLA DOCUMENT READER	ASSOCIATED EQUIPMENT
NO CARD FEED	Defective lamps in sensing head Dirt/foreign objects in sensing head Card Feed board defective FEED switch defective Filler Plate switch defective Loose/broken belts Drive/Idler roller adjustments	Data Set • 40 second delay not completed • Reverse Channel signal missing • Data Set unplugged
BAD DATA	Drive rollers dirty Sensing head dirty Loose belts Card skews (Idler roller adjustment) Card hitting edge of card catcher Hold down spring adjustment Loose board/connector Sensitivity adjustments Bit Oscillator board Timing & Control Logic board	Operator • CARD/PAGE switch in wrong position Documents • Improper markings or punches • Bad format Interface Equipment • Interface device inoperative
CARD JAM	Hopper Gate adjustment Drive/Idler rollers dirty Hold down spring adjustment Foreign objects in sensing head area Drive/Idler roller adjustment	Documents Bent/mutilated cards Operator • Card Eject code entered on card too soon (column 24 on 80-column format)

Table 8. Common Problems Encountered on Service Call

(5) To assemble, perform Steps G. 11. a and b in reverse order.

b. Drive Roller Assembly (10, Fig. 45)

(1) Raise top-rear, hinged portion of housing (39, Fig. 43). Swing to rear of machine.

(2) Verify each drive roller (10, Fig. 45) has a maximum end play of 0.01 inch. End play may be adjusted by repositioning the truarc ring (13) at the end of the shaft.

(3) Release the tension on the drive belt (62, Fig. 44) by loosening the allen screws (59) holding the idler-main bracket (58).

(4) Loosen the four allen screws (3, Fig. 45) which secure the drive frame (7) to the frame (60).

(5) Turn each set screw (9, Fig. 45) counter-clockwise until the top of the screw is flush with drive frame casting (7).

(6) Center the drive rollers (10, Fig. 45) over the idler rollers (43, Fig. 44), as shown in figure 32. While applying a downward pressure, tighten the four allen screws (3, Fig. 45) to hold the drive frame in position, yet still allow movement to the frame using the two set screws (9, Fig. 45).

(7) Take up slack on drive belt (62, Fig. 44) and tighten allen screw (59) in elongated hold of idler-main bracket (58).

NOTE

Do not apply normal belt tension; simply take up slack in belt.

(8) While rotating idler roller (43, Fig. 44), turn corresponding set screw (9, Fig. 45) clockwise until a slight drag is present. Repeat for each roller.

(9) Tighten the four allen screws (3, Fig. 45).

(10) Release tension on drive belt (62, Fig. 44).

(11) Rotate drive rollers in direction of card travel. Verify idler rollers rotate.

(12) Examine drive rollers (10, Fig. 45) for "flat tire" effect at point of contact with idler rollers as shown in figure 32. When adjusted properly, there will be a very slight "flat tire" effect. This insures line-to-line contact.

(13) Manually feed a card through the rollers. Verify card does not bind.

(14) Replace drive belt and adjust per Step F. 1.1.

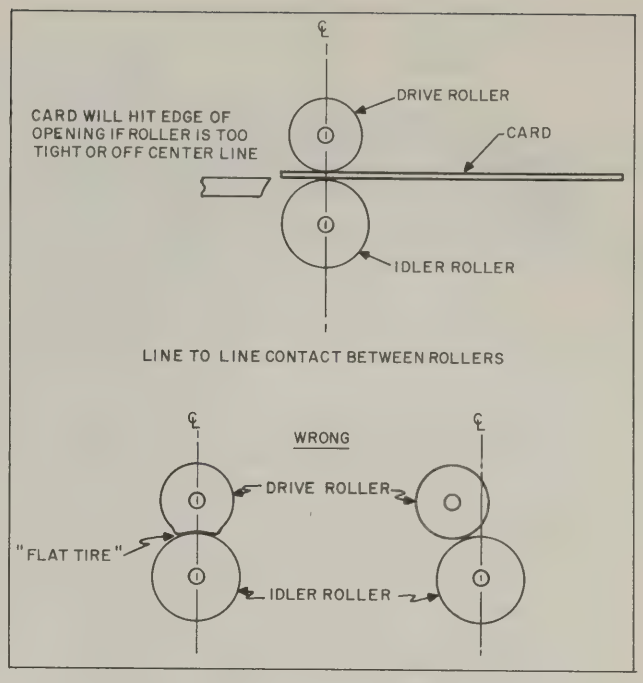


Figure 32. Correct Roller Alignment

c. Hold Down Spring (29, Fig. 45)

(1) Remove data sensor assembly (Paragraph G.16.a thru G.16.i).

(2) With the hold down spring secured to the data sensing assembly, verify all the fingers are parallel to each other as shown in Figure 33.

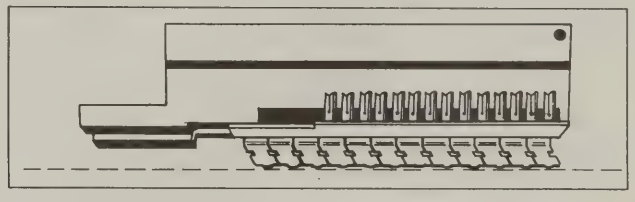


Figure 33. Parallel Alignment of Fingers

CAUTION

Fingers are fragile; therefore, apply only a slight pressure to fingers when aligning. If necessary, repeat pressure several times to position finger properly.

(3) Position sensing head so phototransistors can be observed. Verify the hold down spring does not block or partially block any of the phototransistors (Refer to Figure 34).

(4) If adjustment is necessary, loosen the three positioning screws (30, Fig. 45) on the side of data sensor (26). Position hold down spring and tighten screws.

(5) Replace and secure sensing head assembly.

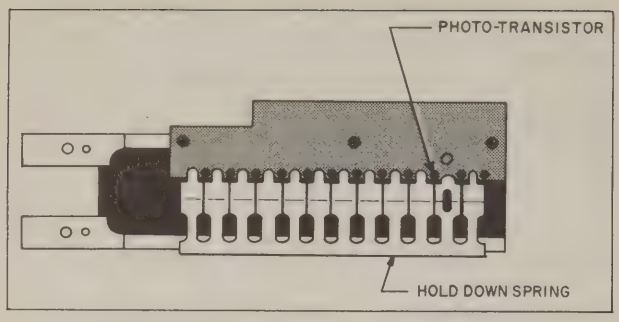


Figure 34. Correct Alignment of Hold Down Spring

(6) Slide a strip of card stock (about the width of three of the fingers) between the hold down spring and the frame (60).

(7) Verify an equal amount of drag is applied to the card stock by each group of fingers.

(8) Manually feed a card into unit; verify the fingers on the hold down spring are approximately flat as shown in Figure 35.

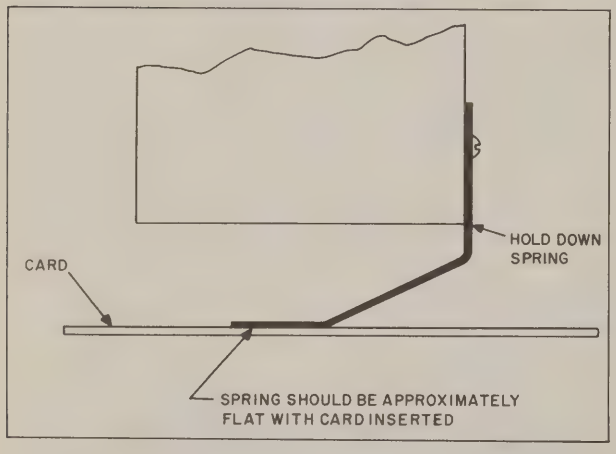


Figure 35. Position of Fingers with Card Inserted

(9) If either step (7) or (8) above fail, perform step (4) again being careful not to move the hold down spring in a horizontal direction.

(10) With the card removed, the fingers of the hold down spring should just barely contact the frame.

d. Sensing Head (25 thru 32, Fig. 45)

The following test equipment is required to accurately align the sensing head:

- Oscilloscope with external triggering capabilities and dual trace (if available).
- Keypunched tab cards containing the letter "I" ("12" and "9" data rows) punched in first ten columns. Card Eject ("12" and "11" data rows) code may be punched in column 24 to speed up alignment procedure. Cards should be verified using an IBM Registration Gauge.

(1) Insert cards in hopper and enable unit.

(2) Connect sync and voltage probe to RED (2nd pre-card program code) wire on the top of the masterboard. Set sweep rate so face of scope will display a 500 millisecond time interval. (Refer to Figure 36).

(3) Press FEED switch. Sync scope on positive signal that is generated by leading edge of card entering read head.

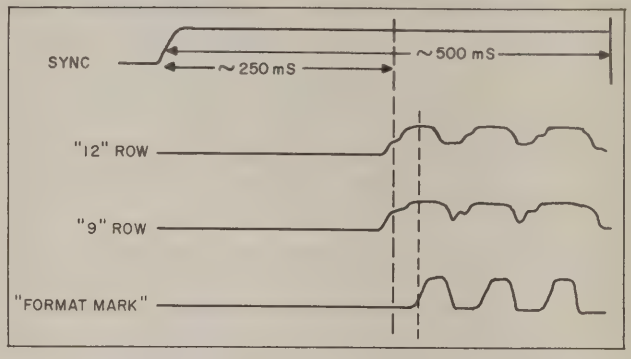


Figure 36. Waveform Outputs of Aligned Sensing Head

(4) Move voltage probe to P13-2 ("12" data row). Observe time that phototransistor detects data. (Refer to Figure 36).

(5) Move voltage probe to P13-13 ("9" data row). Observe time that phototransistor detects data. (Refer to Figure 36).

(6) Move voltage probe to P13-14 (format mark). Observe time that phototransistor detects format mark. (Refer to Figure 36).

Ideally, the "12" and "9" data row signals will occur at the same time. The format mark signal will occur when the "12" and "9" signals are saturated, but prior to the time that the signals begin to decay.

(7) To align sensing head, loosen the two allen screws (25, Fig. 45). Move sensing head slightly. Tighten screws (25) and repeat steps (3) thru (6). Repeat this procedure until sensing head is properly aligned.

e. Card Feed Clutch Assembly (15 thru 29, Fig. 44)

(1) Perform Steps G. 11.a, b, and c.

(2) Release clutch (20, Fig. 44) by lifting stop on solenoid. (Refer to Figure 37).

(3) Rotate main drive gear (69, Fig. 44) clockwise to gain access to set screws on outer ring of clutch assembly. Loosen set screws when accessible.

(4) Continue rotating main drive gear (69) until plastic stop on clutch assembly engages with the solenoid stop. (Clutch will stop rotating.)

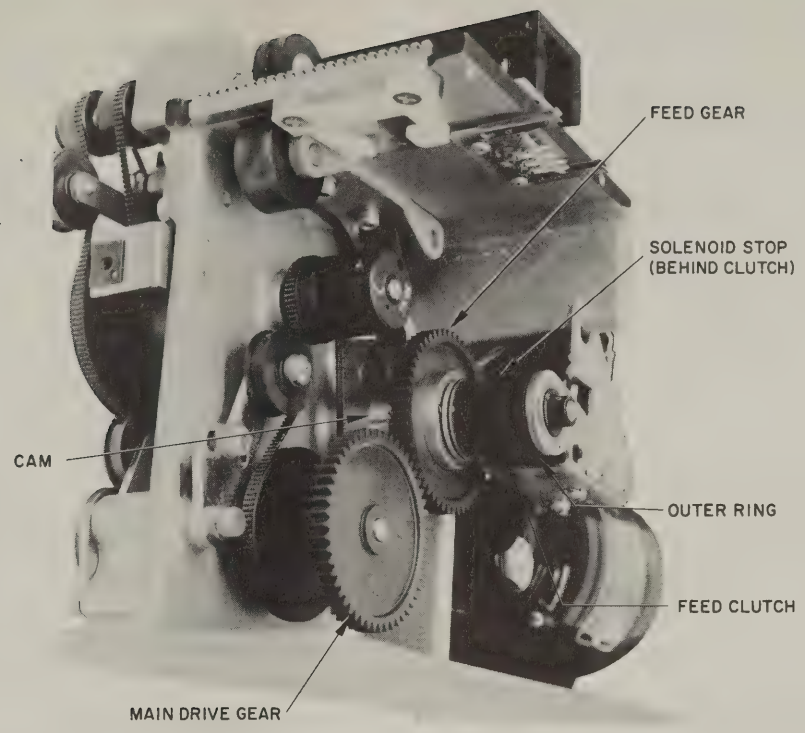


Figure 37. Card Feed Clutch Alignment

(5) Rotate feed roll pulley (10, Fig. 44) in direction of card travel until cam (16) just starts to raise trip bracket (25). (Refer to Figure 37).

(6) Trip solenoid stop and rotate main drive gear (69, Fig. 44 in clockwise direction until over-travel pin in outer ring of clutch assembly (20) is visible. (Refer to Figure 38).

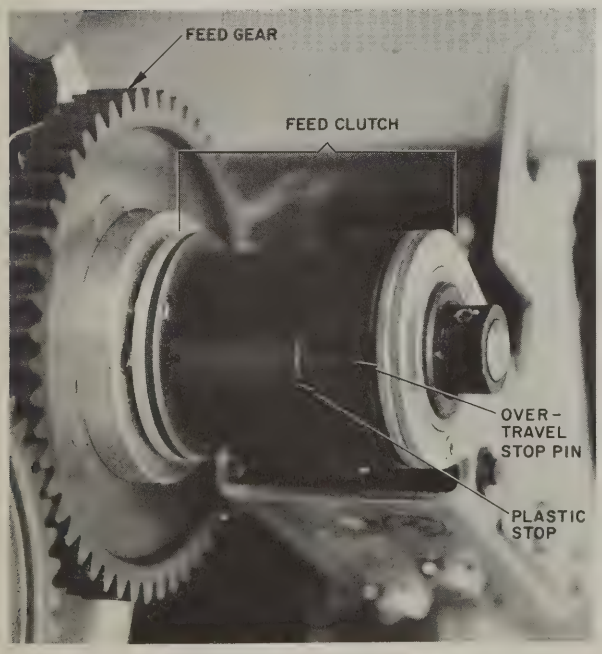


Figure 38. Over-travel Stop Pin Alignment

(7) Position over-travel stop pin in center of dwell. Tighten set screws on outer ring. Continue rotating clutch assembly (20) using main drive gear (69) until plastic stop engages with solenoid stop.

(8) Verify adjustment by releasing solenoid stop. Rotate main drive gear (69, Fig.44) clockwise. Insure trip bracket (25) raises immediately.

(9) Verify feed roll assembly adjustment per Step F. 1. f.

f. Feed Roll Assembly (8, Fig. 44)

(1) Remove hopper (5, Fig. 43).

(2) Place a straight edge over feed roll assembly (8, Fig. 44). Insure straight edge is resting on the raised, machined portion of frame (89). (Refer to Figure 39).

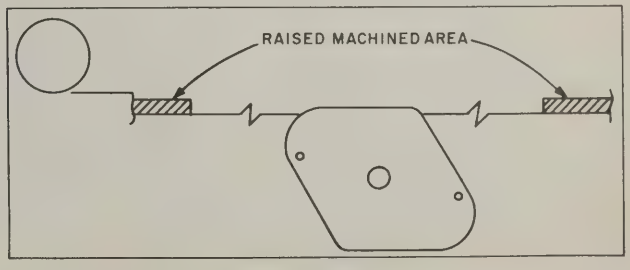


Figure 39. Feed Roll Assembly Alignment

(3) The feed roll assembly (8, Fig. 44) should be almost parallel to the straight edge. Proceed to Step (4) if adjustment is required.

(4) Loosen the two allen screws (11, Fig..44) in the drive pulley (10).

CAUTION

Do not attempt to adjust the feed roll assembly (8) on the shaft (5) since there is only one flat spot on the shaft where the feed roll assembly can be secured.

NOTE

Insure machine is completely cycled before making adjustment. Rotate drive pulley (10, Fig. 44) in a clockwise direction. If machine is properly cycled, drive pulley will be locked in place.

(5) Position the feed roll assembly parallel to the straight edge. Tighten the allen screws (11).

(6) End play for shaft should not exceed 0.010 inch.

(7) Restore unit to operating condition.

g. Eject Clutch (38, Fig. 44)

(1) Perform Steps G. 11. a, b, and c.

(2) Lift trip bracket (Refer to Figure 40). Rotate main drive gear (69) clockwise until set screws on plastic, stop collar in center of clutch (38) are accessible..

(3) Loosen set screw.

(4) Move plastic, stop collar until over-travel stop pin is positioned in center of dwell on the outer ring of the clutch (38). (Refer to Figure 38). Tighten set screw when centered.

(5) Position clutch assembly to observe over-travel stop pin. Rotate stop collar counterclockwise until over-travel pin contacts edge of dwell.

(6) Release stop collar. Over-travel stop pin should return (spring back) to center of dwell.

(7) Rotate stop collar clockwise. Over-travel stop pin should not contact edge of dwell if properly adjusted.

(8) Return unit to normal operating condition.

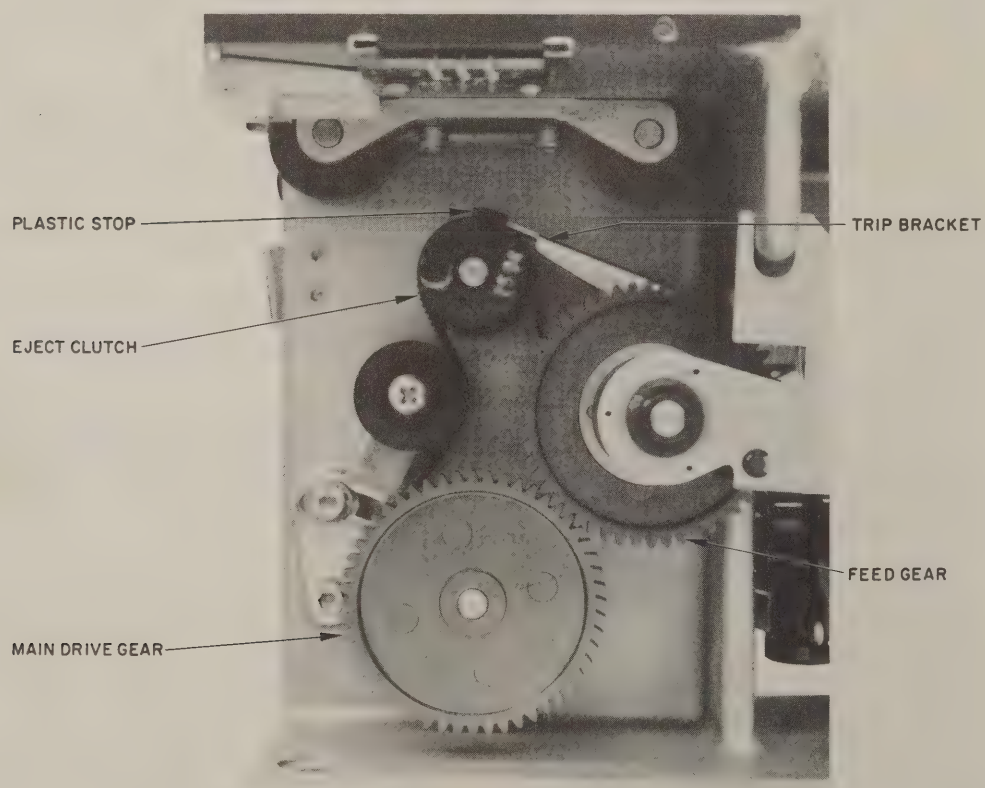


Figure 40. Eject Clutch Alignment

h. Hopper Card Gate (7, Fig. 43)

(1) Using a feeler gauge, verify the clearance of the card gate is 0. 010 +0. 000 -0. 001. Be sure to check the entire width of the card gate.

(2) To adjust the card gate, loosen the two set screws (8, Fig. 43). Adjust clearance and tighten set screws. Insure card gate is parallel to base plate by running feeler guage the width of card gate.

i. Filler Plate Switch S7 (53, Fig. 44)

(1) Remove filler plate or hopper.

(2) Place a straight edge over the switch and press down until the straight edge is flush with the frame (89). The switch should enable (audible) while pressing down on the straight edge..

(3) To adjust, loosen the two mounting nuts (54). Raise or lower the switch as required.

NOTE

The threads on the switch should not extend above the frame.

(4) Tighten the mounting nuts and verify adjustment by repeating step (1) above.

j. Hopper Empty Switch S6 (46, Fig. 44)

(1) With the hopper (5, Fib. 43) in place and the button actuator (9) depressed, the switch should enable (audible).

(2) To adjust, loosen the four mounting screws (52, Fig. 44) and remove the switch assembly.

(3) Adjust the positioning screws (49, Fig. 44) and nuts (51) to either raise or lower the switch with respect to the mounting brackets (47, 48).

(4) Install switch assembly, tighten mounting screws, and verify adjustment by repeating Step (1) above.

k. Idler Roller Assembly (43, Fig. 44)

(1) Perform Steps G. 11. a, b, and c.

(2) Loosen the two allen screws (44, Fig. 44) and turn the idler roller assembly so that the rollers will force a card against the drive frame guide as shown in Figure 41.

(3) Tighten the two allen screws (44, Fig. 44).

(4) Apply power to Document Reader. Feed a card into drive rollers (10, Fig. 45).

(5) Verify card is forced against guide ridge without buckling card.

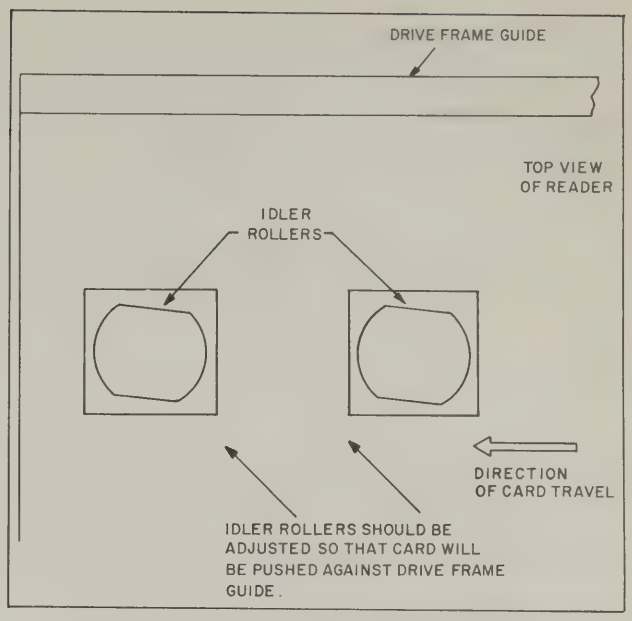

DRIVE FRAME GUIDE
TOP VIEW OF READER
IDLER ROLLERS
DIRECTION OF CARD TRAVEL
IDLER ROLLERS SHOULD BE ADJUSTED SO THAT CARD WILL BE PUSHED AGAINST DRIVE FRAME GUIDE.

Figure 41. Idler Roller Assembly Alignment

(6) Verify the drive roller assembly adjustment is still correct (refer to Paragraph F. 1. b).

(7) Restore unit to operating condition.

l. Belt Tensions

Adjust belts to the following tensions:

Belt	Reference	Tension
Motor drive belt	55, Fig. 44	3 to 3-1/2 lbs
Roller drive belt	62, Fig. 44	3 to 3-1/2 lbs
Eject roller drive belt	40, Fig. 44	3 to 3-1/2 lbs
Eject drive belt	34, Fig. 44	4 to 4-1/2 lbs
Timing belt	4, Fig. 44	Take up slack

(1) Motor Drive Belt (55, Fig. 44)

(a) Loosen the shoulder screw (34, Fig. 45)

(b) Using a tension gauge (Chatillon #767), grasp the extended portion of the idler-motor bracket (33, Fig. 45) and raise idler-motor bracket by the gauge. When a reading of 3 to 3-1/2 lbs. is indicated on the gauge, tighten the shoulder screw (34).

(2) All Other "V" Belts

(a) Loosen both screws securing the respective idler bracket.

(b) Place a tension gauge (Chatillon #767) against screw securing the pulley to the idler bracket and apply tension in direction of belt.

(c) When gauge indicates the proper tension,

tighten the allen screw in the elongated hole; then, secure the pivot screw.

(3) Timing Belt (4, Fig. 44)

(a) Loosen both screws (50, Fig. 45) securing the idler-feed bracket (49).

(b) Using thumb, apply enough tension against idler-feed bracket to remove slack in belt. Tighten allen screws (50, Fig. 45).

2. Electrical Adjustments And Test Points

a. Fuses

Location	Designation	Description
On rear of machine	F1	MAIN - 117 Vac, 3AG, 3A
On lower front portion of power supply	PS1F1	MOTOR - 117 Vac, 3AG, 3A
On front of power supply	PS1F2	IC - +5.0 Vdc, 3AG, 3A
On front of power supply	PS1F3	COMP - +12 Vdc, 3AG, 5A
On top of power supply	PS1A1F1	LAMP - 15 Vdc, 3AG, 3A

b. Power Supply

Connect ground lead from scope or meter to power common. Power common is available at the positive side of any of the electrolytic capacitors (PS1A1C1, -C2, -C3, or -C4) on the lamp power supply circuit board PS1A1.

CAUTION

The chassis not connected to power common. Adjusting voltages using chassis ground will cause fuses to blow.

(1) Lamp Supply PS1A1

(a) Connect test probe to center pin of sensor lamp connector P12 (24, Fig. 45).

(b) Verify a maximum voltage of ~~17.0~~ 16.2 VDC Vdc. LAMP VOLTAGE potentiometer PS1A1R4 (top of lamp supply circuit board) can be adjusted for proper reading.

(2) IC Supply PS1A2

(a) Connect test probe to top bus bar on the rear of card cage (63, Fig. 43).

(b) Verify a voltage reading of +5.0 ±0.1 Vdc. Adjust VOLTAGE potentiometer PS1A2R7 to obtain the proper reading. Potentiometer is accessible through labelled hole in the lamp supply board.

NOTE

If IC fuse PS1F2 blows, adjust potentiometer fully counterclockwise; replace fuse. Then, make adjustment.

(3) Component Supply PS1A3

(a) Connect test probe to connector J3, pin 3 (two orange wires.)

(b) Verify voltage reading of +12.0 ±1.5 Vdc.

NOTE

There is no adjustment for this power supply. If voltage is out of tolerance, a component malfunction exists.

c. Sensitivity Adjustments

(1) Format Clock

(a) Connect test probe to connector P13, pin 14 (pin closest to card cage).

(b) Verify a voltage reading of 1.0 ±0.1 1.2 to 1.5 VDC Vdc. FORMAT CLOCK potentiometer A1A2R3 (Location No. 2 - potentiometer nearest master board) may be adjusted to obtain proper reading. Clockwise rotation decreases sensitivity; counterclockwise increases sensitivity.

(2) Trailing Edge

(a) Connect test probe to connector P14, pin 2 (left-most pin on L/T sensor - Item 1, Fig. 44).

(b) Verify voltage reading of 1.0 ±0.1 Vdc.

(c) Insert card under read head; verify voltage reading of 4.0 Vdc or greater. TRAILING EDGE potentiometer A1A2R15 (Location No. 2 - center potentiometer) may be adjusted to obtain proper reading. Clockwise rotation decreases sensitivity; counterclockwise increases sensitivity.

(3) Leading Edge

(a) Connect test probe to connector P14, pin 1 (right-most pin on L/T sensor - Item 1, Fig. 44).

(b) Verify voltage reading of 1.0 ±0.1 Vdc.

(c) Insert card under read head; verify voltage reading of 4.0 Vdc or greater. LEADING EDGE potentiometer A1A2R9 (Location No. 2 - potentiometer nearest

end of board) may be adjusted to obtain reading. Clockwise rotation decreases sensitivity; counterclockwise increases sensitivity.

(4) Data Rows 1 thru 12

(a) Connect test probe to connector P13, pins 2 thru 13. (Do not connect to end pins on phototransistor board.)

(b) Verify voltage reading of 1.0 ±0.1Vdc.

(c) Insert marked card under read head; verify voltage reading of 4.0 Vdc or greater when mark is detected. SENSITIVITY potentiometer A1AIR73 (Location No. 1) may be adjusted to obtain proper reading. Clockwise rotation decreases sensitivity; counterclockwise increases sensitivity.

G. DISASSEMBLY

CAUTION

Before proceeding with any maintenance, turn power off, unplug power cord, and disconnect any external connection to output connector J15.

1. Removal of Card Receiver (1, Fig. 43)

a. Grasp card receiver

b. Pull down and away from machine.

2. Removal of Filler Plate (4, Fig. 43)

a. Insert finger tips under right-hand side of filler plate.

b. Lift up until plate unlatches; then, remove plate.

3. Removal of Hopper (5, Fig. 43)

a. Insert finger tips under right-hand side of hopper.

b. Lift up until hopper unlatches; then, remove hopper.

4. Removal of Cover Plate (11, Fig. 43)

a. Raise top-rear hinged portion of the housing (39). Swing to the rear of the machine.

b. Depress right- and left-hand retaining latches on each side of cover plate..

c. Slide cover plate to the front of the machine and lift off.

5. Removal of the Housing Cover (12, Fig. 43)

a. Perform Steps 1 and 4.

b. Remove the two (hand tight) cover plate mounting studs (13).

c. Remove phillips screw and washer (15, 16) from each side of the housing cover.

d. Grip the housing cover on each side and raise up at the same time. Lay housing cover out to the front of the machine upside down.

e. Separate cable connectors J4 and J6 (54, 60) from the housing cover. Lay housing cover aside.

6. Removal of Operator's Panel

a. Perform Steps 1, 4 and 5.

b. Remove nuts and washers (17, 18 or 28,29) from underside of housing cover. Parts may now be replaced on this assembly.

7. Replacement of Indicator Lamps (20 or 31, Fig. 43)

a. For Operator's Panel Using Lamp 20 Configuration

(1) Perform Steps 1, 4 and 5.

(2) Separate terminal board (19) from PWB assembly (21).

(3) Remove lamp (20).

b. For Operator's Panel Using Lamp 30 Configuration

(1) Grasp indicator cover (30) and pull up.

(2) Using fuse puller, grasp lamp (31) and pull up to remove lamp.

8. Removal of Rear Plate (40, Fig. 43)

a. Raise top-rear portion of the housing (39). Swing to the rear of the machine.

b. Lift the air duct housing (70) off the four guide studs (19, Fig. 46) on the rear of the power supply (75, Fig. 43). Lay air duct aside.

c. Remove four mounting screws (41) and speed nuts (42) from the rear plate..

NOTE

Although several wire connections exist, the rear plate may be extended from the housing for further maintenance.

9. Removal of Card Cage Assembly (63, Fig. 43)

a. Perform Steps 1, 4 and 5.

b. Separate cable connectors P5 and J5 (66, 56).

c. Remove cable connectors P9 and P10 (49, 61) from the card cage (63).

d. Disconnect L/T sensor connector P14.

e. Remove circuit boards from Locations No. 2 and No. 1 (in that order) from card cage.

f. Remove the screw and washer (64, 65) from each corner of the card cage.

g. Lift the card cage assembly up and to the front of the machine.

10. Removal of Circuit Boards From Card Cage Assembly (63, Fig. 43)

a. Perform Step 1.

b. Depress the right- and left-hand retaining latches on the cover plate (11).

c. Slide the cover plate (11) to the front of the machine and lift out.

d. Select the circuit board to be removed. Grip the top of the circuit board; pull up and then towards the center of the machine. Carefully lift board out when free of the connector. (Refer to Figure 42)

11. Removal of Drive Mechanism Assembly (67, Fig. 43)

a. Perform Steps 1, 2, (or 3), 4 and 5.

b. Tip unit on its side, install service feet, and remove the four mounting pads (81, 82, 83, Fig. 43). With unit in normal operating position, base plate (80) will be raised above edge of housing (39).

c. Remove circuit boards from card cage, Locations No. 4, 3, 2 and 1 in that order.

d. Disconnect cable connector P7 (59, Fig. 43) from the drive mechanism (67).

e. Disconnect cable connector J8 (39, Fig. 45) at the motor (38).

f. Disconnect the orange wire from audible alarm DS1 (71, Fig. 43).

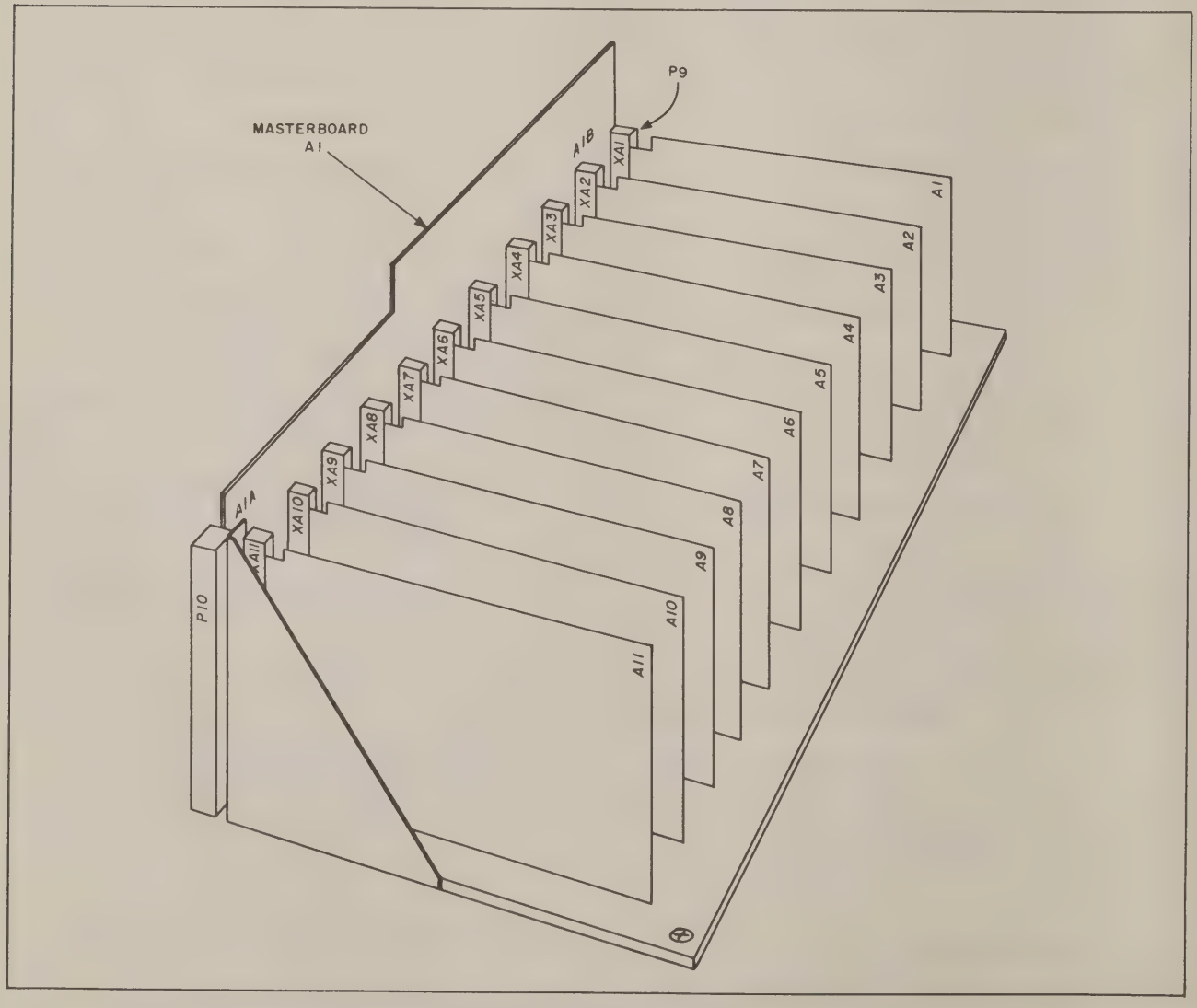


Figure 42. Card Cage Layout

Legend for Figure 42.

Identification	Board Part Number	
	Serial Output Unit	Parallel Output Unit
MASTERBOARD	01-F7891G01	01-F7789G01
Location XA1		
Data Amplifier	01-F7870G01	01-F7870G01
Location XA2		
L/T & Clock Amp	01-F7871G01	01F7871G01
Location XA3		
Data Register	01-F7873G01	01F7873G01
Location XA4		
USASCII 15 Char	01-F7869G01	01-F7869G01
USASCII 85 Char	01-F7874G01	01-F7874G01
PTTC/BCD	01-F7784G01	01-F7784G01
EBCDIC	01-F7782G01	01-F7782G01
HOLLERITH	N.A.	01-F7785G01
Location XA5		
USASCII 15 Char	None	None
USASCII 85 Char	01-F7875G01	01-F7875G01
PTTC/BCD	None	None
EBCDIC	01-F7783G01	01-F7783G01
HOLLERITH	N.A.	None
Location XA6		
USASCII 15 Char	None	None
USASCII 85 Char	01-F7876G01	01-F7876G01
PTTC/BCD	None	None
EBCDIC	None	None
HOLLERITH	N.A.	None
Location XA7		
Timing & Control		
Logic	01-F7877G01	01-F7786G01
Location XA8		
Data Out-Phone	01-F7878G01*	N.A.
Data Out - TTY	01-F7880G01*	N.A.
Interface Driver	N.A.	01-F7788G01
Location XA9		
Manual Feed	None	None
Automatic Feed	01-F7884G01	01-F7884G01
Location XA10		
No Options	None	N.A.
Hopper Empty	01-F7888G01	N.A.
Alarm & BEL	01-F7886G01	N.A.
Reader Cont		
Interface	N.A.	01-F7787G01
Location XA11		
TTY Control	None	N.A.
Phone Cont-Unatt	01-F7889G01	N.A.
Phone Cont - Att	01-F7890G01	N.A.

*Board contains plug-in Bit Oscillator. Part Number for Bit Oscillator will depend upon transmission speed of unit. For 105 bits/second, part number is 01-F7882G01; for 1050 bits/second, part number is 01-F7882G02.

g. Disconnect P15 (wire to HORN switch S4 (73, Fig. 43 on rear plate (40) if used.

h. Disconnect cable connector P9 (49, Fig. 43)

i. Remove screws and washers (68, 69) from each corner of drive mechanism.

j. Remove the drive mechanism (67) from the base plate.

12. Removal of Power Supply PSl (75, Fig. 43)

a. Perform Steps 1, 2 (or 3), 4 and 5.

b. Remove circuit boards from card cage, Locations No. 4, 3, 2 and 1, in that order.

c. Tip unit on side. Insert service feet into underside of unit. Remove mounting pads (81, 82, 83).

d. Position unit in normal operating position. Base plate (80) will be raised above lip of housing.

e. Lift the air duct housing (70) off the four guide studs (19, Fig. 46) on the rear of the machine

f. Disconnect cable connectors Pl, P2, and P3 (53, 57, and 58) from the power supply.

g. Remove the three screws and washers and the post (76, 77, 78, and 79) holding the power supply to the base plate (80).

h. Remove the power supply.

13. Removal of Sensor Lamp Assembly (1, Fig. 45)

a. Raise top-rear hinged portion of the housing (39, Fig. 43). Swing to the rear of the machine.

b. Grasp the sensor lamp assembly and pull it straight out of the data sensor assembly (26, Fig. 45)

14. Removal of Drive Roller Frame Assembly (3 thru 18, Fig. 45)

a. Raise top-rear, hinged portion of the housing (39, Fig. 43) Swing to rear of the machine.

b. If used, release the skip-idler bracket (19, Fig. 45) by loosening the two allen screws (20). Remove the skip drive belt (18).

c. Release main-idler bracket (58, Fig. 44) by loosening allen screws (59). Remove main drive belt (62).

d. Remove allen screws, washers, and the cable clamp (3 thru 6, Fig. 45) that retain the drive frame assembly to the frame.

e. When assembling, see paragraph F. 1. b. for adjustments.

15. Removal of Drive Roller (10, Fig. 45)

a. Raise top-rear, hinged portion of the housing (39, Fig. 43). Swing to rear of machine.

b. If used, release the skip-idler bracket (19, Fig. 45) by loosening the two allen screws (20). Remove skip drive belt (18).

c. Release the main-idler bracket (58, Fig. 44) by loosening two allen screws (59). Remove main drive belt (62).

d. Remove truarc ring (13, Fig. 45) at end of drive roller (10).

e. Carefully remove each part (14, 15, 17, 12, and 15) from the end of the shaft (10). Keep parts in order for assembly.

f.. Remove drive roller and spacer (10, 11) from drive frame (7)

NOTE

Bearing (8, Fig. 45) will not separate from drive frame (7). To remove bearings, insert punch into shaft opening and drive bearing out of frame.

g. When assembling, see paragraph F. 1. b for adjustments.

16. Removal of the Data Sensor Assembly (26, Fig. 45)

a. Raise top-rear hinged portion of the housing (39, Fig. 43). Swing to the rear of the machine.

b. Grasp the sensor lamp assembly (1, Fig.. 45) and pull it out of the data sensor assembly (26).

c. Remove the phillips screw (44, Fig. 43) and washer (45) that retain the sensor cable.

d. Remove the phillips screw (47) and washer (48) that retain connector P13 (51) to the data sensor assembly.

e. Carefully raise connector P13 (51, Fig. 46) separating it from the phototransistor board (27, Fig. 45)

f. Remove the phillips screws (23, Fig. 45) that retain connector P12 (24) to the data sensor assembly (26).

g. Remove connector P12 (24).

h. Remove the two allen screws (25) to separate the data sensor assembly from the frame (60).

i. Raise the data sensor assembly over the two aligning pins and remove.

j. To remove the hold down spring (29), remove the phillips screws (30) and washer s, (31, 32) from the data sensor.

k. To remove the phototransistor board (27), remove the three phillips screws (28) from the data sensor.

l. When assembling, see paragraphs F. 1. c and F. 1. d for adjustments.

17. Removal of L/T Sensor Assembly (1, Fig. 44)

a. Perform Step 1.

b. Depress the right- and left-hand retaining latches on each side of the cover plate (11, Fig. 43).

c. Slide cover plate to the front of the machine and lift off.

d. Unplug connector plug P14 (50, Fig. 43).

e. Remove circuit boards from Locations No. 1 thru 7 of card cage (63, Fig. 43). Grip rear top of board; pull up and toward center of the machine. Carefully lift board out.

f. Remove the phillips screws (2, Fig. 44) and washers (3).

18. Removal of the Clutch Shaft and Trip Bracket Assemblies (15 thru 29, Fig. 44) or Feed Roll Assembly (8)

a. Perform Steps 1, 2 (or 3), 4, 5, and 9.

b. Remove feed roll pulley (10, Fig. 44) hopper drive pully (12), and drive timing belt (4) by loosening the set screws (11, 13) in the pulleys.

c. To remove the Clutch Shaft and Trip Bracket Assemblies:

(1) Remove the two wires from the clutch solenoid (20).

(2) Raise the trip bracket (25) to clear cam (16) and remove the clutch chaft assembly.

(3) To remove the trip bracket assembly (25), remove the phillips screw (26) and washer (27).

d. To Remove the Feed Roll Assembly:

(1) Loosen the two set screws (9) in the feed roll assembly (8).
(2) Replace the feed roll pulley (10) and tighten set screw (11).

(3) Using the feed roll pulley as a knob, remove feed roll shaft (5).

NOTE

Be careful not to drop washer (7) when removing feed roll assembly (8) from frame.

e. When assembling, see paragraphs F. 1. e and f for adjustments.

19. Removal of Skip Feed Clutch (38, Fig. 44) and Clutch Shaft (35)

a. Perform Step 1.

b. Raise top-rear hinged portion of the housing (39, Fig. 43). Swing to the rear of the machine.

c. Depress the right- and left-hand retaining latches on each side of the cover plate (11).

d. Slide cover plate to the front of the machine and lift off.

e. Release the idler bracket (30, Fig. 44) by loosening the allen screws (31).

f. Loosen the set screw (39) that retains the skip feed clutch (38) on the shaft (35).

g. Remove the drive belt (34) from the skip feed clutch; then, remove the skip feed clutch assembly.

NOTE

When assembling, insure set screw (39, Fig. 44) is tightened on flat portion of shaft.

h. Release the idler-skip arm assembly (19, Fig. 45) by loosening the allen screws (20).

i. Remove belt (40, Fig. 44).

j. Grasp pulley (41) and remove clutch shaft (35) and pulley (41) from frame (89).

k. When assembling, see paragraphs F. 1. e, f, and g for adjustments.

20. Removal of Motor (38, Fig. 45)

a. Perform Steps 1, 2 (or 3), 4, 5, and 12.

b. Release idler-motor bracket assembly (33, Fig. 45) by turning shoulder screw (34) counterclockwise.

c. Remove drive belt (44, Fig. 45).

d. Remove motor shaft pulley (45, Fig. 45) by loosening set screw (46).

e. If used, remove motor shaft adapter (47, Fig. 45) by loosening set screw (48).

f. Remove the four motor mounting screws (37, Fig. 45) from mounting plate (40).

NOTE

When removing motor, note position of power cable for assembly.

g. Rotate motor as necessary for removal.

h. When assembling, see paragraph F. 1. a for adjustment.

21. Removal of the Idler Roller Assembly (43, Fig. 44)

a. Perform Steps 11. a, b and c.

b. Remove the two allen screws (44, Fig. 44) and washers (45) that retain the idler roller assembly (43) to the frame (89).

c. When assembling, see paragraph F. 1. k for adjustments.

22. Removal of the Hopper Empty Switch S6 (46, Fig. 44)

a. Perform Steps 1 and 4.

b. Remove the four phillip screws (52, Fig. 44) from the switch mounting bracket (47, 48).

c. Lift the switch assembly from the machine; tag, and unsolder the attaching wires.

d. When assembling, see paragraph F. 1. j for adjustments.

23. Removal of the Filler Plate Switch S7 (53, Fig..44)

a. Perform Steps 1, 2 (or 3), 4,5, 9, and 11.

b. Unscrew the retaining nut (54, Fig. 44) and remove the switch from the drive mechanism.

c. Tag and unsolder the attaching wires.

d. When assembling, see paragraph F. 1. i for adjustments.

24. Removal of Main Shaft (68, Fig. 44)

a. Perform Steps 1, 4, 5, and 9.

b. Release the idler-motor bracket assembly (33, Fig. 45) by turning the shoulder screw (34) counterclockwise.

c. Remove the drive belt (44).

d. Release the idler-main bracket assembly (58, Fig. 44) by loosening the allen screws (59).

e. Remove shaft pulley (56) by loosening the set screw (57).

f. Remove the main shaft pulley (63) by loosening the set screw (64).

g. Release idler-skip bracket assembly (30) by loosening allen screws (31).

h. Remove shaft (68), pulley (65), and gear (69).

i. Return unit to proper operating condition.

25. Removal of Belts

a. Motor Drive Belt (55, Fig. 44) (44, Fig. 45)

(1) Release idler bracket assembly (33, Fig. 45) by turning shoulder screw (34) counterclockwise.

(2) Remove belt from pulleys (45, Fig. 45) and (56, Fig. 44).

b. Hopper Feed Timing Belt (4, Fig. 44)

(1) Release idler-feed bracket (49, Fig. 45) by loosening allen screws (50).

(2) Free feed roll pulley (10, Fig. 44) and hopper drive pulley (12) by loosening set screws (11, 13) in the pulleys.

(3) Remove timing belt, and pulleys simultaneously.

c. Skip Drive Belt (40, Fig. 44) (18, Fig. 45)

(1) Release idler-skip arm assembly (19, Fig. 45) by loosening allen screws (20).

(2) Remove skip drive belt from clutch pulley (17).

d. Drive Belt (62, Fig. 44) (16, Fig. 45)

(1) Perform Step 25a.

(2) Release idler-main bracket (58, Fig. 44) by loosening allen screws (59).

(3) Remove drive belt.

e. Skip Clutch Drive Belt (34, Fig. 44)

(1) Release idler-skip bracket (30, Fig. 44) by loosening allen screws (31).

(2) Raise trip bracket assembly (25, Fig. 44) and remove belt from clutch pulley (38) and main shaft skip pulley (65).

(3) Perform Step 25a and 25d.

(4) Refove shaft pulley (56) by loosening set screw (57).

(5) Remove main shaft pulley (63) by loosening set screw (64).

(6) Push main shaft assembly outward until gears (69, 18) unmesh.

(7) Remove skip clutch drive belt.

H. FINAL SYSTEM OPERATIONAL CHECK

Generally, inspect the unit for cleanliness, specifically in and around the sensing head. Check the drive belts for wear, the power cord for cracks or loose connections, the drive rollers and idler rollers for cleanliness, and all mechanical parts for security.

Restore the unit to its normal operating condition, and then perform the customer's normal operation. Verify the documents feed properly in manual mode, and automatic mode.

In case of a service call, perform the operation that originally initiated the service call. This will validate to the customer's satisfaction that the problem is solved.

Generally, run through the entire operational capabilities of the unit. In many instances, this will prevent another service call.

I. RETURNING DEFECTIVE PARTS

All defective parts returned to Phoenix should use the shipping containers, mailing labels, and report forms available.

The following procedure should be performed when returning a defective part:

1. Enter on the report form the serial number of of the MDR Document Reader.

2. Enter on the report form the serial number of the defective part.

3. Enter on the report form the serial number of the replaceable part installed in the MDR.

4. Complete the report form as required, identifying type of trouble, date, etc.

5. Enclose the report form, a self-addressed mailing label, and defective part in shipping container.

6. Send to:

Motorola Control Systems
P.O. Box 1509
Phoenix, Arizona 85010
ATTN: Service Department

Upon receipt of shipping container, a new part will be immediately returned to the sender, along with new mailing labels, and report form.

J. ON-LINE TESTING PROCEDURE (To Phoenix)

Emergency technical assistance and on-line testing facilities are available from Phoenix, Arizona during the hours of 8:00 a.m. to 4:30 p.m., M.S.T., Monday thru Friday, except holidays.

Before placing a call, have the following information available:

- Model number and serial number of MDR Document Reader
- Type of modem and its model number
- Telephone number of the modem from which the data is going to be sent.

Call: Area Code - 602
Telephone Number 959-1000
Inform operator you wish to be connected to Service Department.

VIII. PARTS LIST (Replaceable Parts Only)

This Parts List includes only those items deemed replaceable in the field. If a piece part fails and is not listed in the Parts List, then the assembly containing the defective part should be ordered.

The "Figure Index Number" column is numerically arranged in the Parts List and is used mainly to assist in location of the part in the Parts List after it has been found in the associated exploded view. (Figures 43, 44, 45 and 46).

A system of compound reference designations is used for describing the electronic module assemblies. All module reference designations are suffixed with the reference designation of the next lower assembly. This, in turn, is suffixed with the reference designation of the next lower assembly. This continues until the reference designation of the lowest assembly or part to be mentioned is included. The reference designations of the modules of the MDR Document Reader are:

Reference Designation	Module
A1	Card Cage Assembly
A2	Leading/Trailing Edge Sensor Assembly
A3	Sensor Assembly
A4	Sensor Lamp Assembly
PS1	Power Supply Assembly

Thus, PS1A2R1 refers to resistor R1 of the IC Power Supply Assembly A2 of the Power Supply Assembly PS1.

The "Motorola Part Number" column is used exclusively to identify parts.

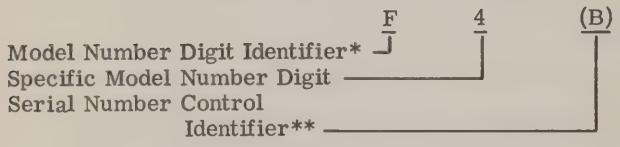
The quantities listed are, in the case of assemblies, the total number used per Document Reader, while the component parts indented under the assemblies are the quantities used per assembly. Therefore, component part quantities are not necessarily the total quantities per Document Reader.

The model number of the MDR Document Reader provides the "key" to the optional features built into the machine. For this reason, a "Usable On Code" column has been incorporated into the replacement parts lists.

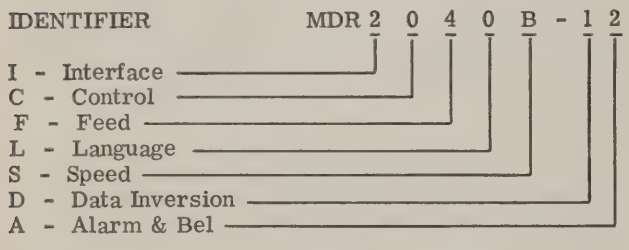
Part variations and options are indicated by a combination of alphanumeric characters in the "Usable On

Code" column immediately preceding the description of the part. An explanation of the alphanumeric characters is outlined below. In cases where the "Usable On Code" column contains only a "-" (hyphen) for an assembly, the assembly and its component parts are used on all document readers covered by this manual.

EXAMPLE LISTING



*MDR MODEL NUMBER DIGIT IDENTIFIER



**SERIAL NUMBER CONTROL IDENTIFIER

Serial Number	Control Identifier
100-134	Under Engineering Control
135-xxx	(A)
xxx and above	(B)

To identify the applicable parts, read and record the model and serial numbers of your machine. For example:

Model Number MDR2040B-12
Serial Number 202

Using the above Model Number and Serial Number as examples, the following "Usable On Codes" in the Parts Lists would apply:

I2 CO F4 L0 SB D1 and A2

The "I2" code is derived from the first digit of the model number, "2" being the specific (actual) digit of the model number, "I" being the "identifier." The "C0" code is derived from the second digit of the model number, "0" being the specific (actual) digit of the model number, "C" being the identifier.

In some cases, "Serial Number Control" may apply to the part. The "Usable On Code" would, then, be modified by the addition of an alpha character enclosed in parentheses (i.e., F4(A)). Consult the Serial Number Control Identifier Listing to determine the codes that effect your machine.

---*---

Figure Index Number	Reference Designation	Motorola Part Number	Qty	Usable On Code	Description
43-		01-F7780G01	1	–	ASSEMBLY, CARD RECEIVER
-1		01DF7364F01	1		. Receiver, card
-2		01CF7533F01	1		. Deflector, card
					/ attaching hardware /
-3		47BF7484H01	1		. Bar, spring
-4		64CF7805G01	1	–	ASSEMBLY, FILLER PLATE
-5		01DF7826G01	1	F2, F4	HOPPER ASSEMBLY, 80-COLUMN
-6		01CF7249F01	1		. Weight, card
-7		45CF7801C01	1		. Gate, card
					/ attaching hardware/
-8		03N46997A22	2		. Screw, socket head, 6-32 x 1/8
					---*---
-9			1		.
					/ attaching hardware /
-10			1		.
-11		15-F7803G01	1	–	ASSEMBLY, COVER PLATE
-		01-F7822G01	1	(B)	COVER ASSEMBLY, HOUSING
-12		15DF7377H01	1		. Cover, housing
					/ attaching hardware /
-13		46BF7306F01	2		. Stud, adjusting
-14		02AF9021H01	4		. Nut, hex, 8-32 x 11/32
-15		03AF9001G06	2		. Screw, phillips, pan head, 6-32 x 3/8
-16		04N45635A02	2		. Washer, flat #6
					---*---
-		64-F7849G01	1		. Assembly, front panel (Include Model Number when ordering)
					/ attaching hardware /
-17		02AF9021G02	6		. Nut, 6-32
-18		64N47976A10	6		. Washer, flat #6
					---*---
-19		31-F7851G01	1		. . Assembly, terminal board
-20	DS1,2,3	65N45397A01	3		. . Lamp, midget flanged, 14V 0.08A, GE330
-21		01-F7850G01	1		. . PWB Assembly, front panel
					/ attaching hardware /
-22		03N46925B33	2		. . Screw, phillips, 4-40 x 1/4
					---*---
-23	S1	40CF7515F03	1		. . Switch, rocker
					/ attaching hardware /
-24		03N46973A36	2		. . Screw, phillips, pan head, 6-32 x 1/4
-25		04N45854B05	2		. . Washer, flat #6
-	P6	28N46907A56	1		. . Connector, 12-pin, Amplok
-	P4	28N46907A53	1		. . Connector, 4-pin, Amplok
-26		40-F7852G01	1	D1 (B)	SWITCH ASSEMBLY
-	S3	40CF7515F04	1		. Switch, rocker
					/ attaching hardware /
-		03N46973A36	2		. Screw, phillips, pan head, 6-32 x 1/4
-		04N45854B05	2		. Washer, flat #6
-		01-F7822G02	1	(A)	COVER ASSEMBLY, HOUSING
-12		15DF7377H01	1		. Cover, housing
					/ attaching hardware /
-13		43BF7306F01	2		. Stud, adjusting
-14		02AF9021H01	4		. Nut, hex, 8-32 x 11/32
-15		03AF9001G06	2		. Screw, phillips, pan head, 6-32 x 3/8
43 -16		04N45635A02	2		. Washer, flat #6
					---*---

Figure Index Number	Reference Designation	Motorola Part Number	Qty	Usable On Code	Description
43-		01-F7824G01	1		. Assembly, front panel
					/ attaching hardware /
-28		02N45468A01	6		. Nut, 4-40 x 1/4
-29		04N45501A01	6		. Washer, flat #4
					---*---
-		54CF7326F	1		. Insert, front panel
					(Include Model Number when ordering.)
-30	DS1,2	09N46946A31	2		. Indicator, lamp assembly - green
-31		65N46952A47	2		. . Lamp, slide base, 6V 35-45 mA, Sylvania 6ESB
-		43B7768B01	1		. Insert, SEND
-		43B7768B03	1		. Insert, READY
-32	DS3	09N46946A32	1		. Indicator, lamp assembly - red
-		65N46952A47	2		. . Lamp, slide base, 6V 35-45 mA, Sylvania 6ESB
-		43BF7768B02	1		. Insert, ALARM
-	P6	28N46907A59	1		. Connector, 6-pin, Amplok
-		40-F7867G01	1	C0(A)	SWITCH ASSEMBLY - UNATTENDED
-	P4	28N46907A53	1		. Connector, 4-pin, Amplok
-33A	S1	40CF7363F02	1		. Switch, rocker
					/ attaching hardware /
-34		02A46698D01	2		. Nut, tubular, 4-40 x 1/2
-35		04N45635A01	2		. Washer, internal lock #4
-		40-F7868G01	1	C1(A)	SWITCH ASSEMBLY - ATTENDED
-	P4	28N46907A53	1		. Connector, 4-pin, Amplok
-33B	S1	40CF7363F01	1		. Switch, rocker
					/ attaching hardware /
-		02A46698D01	2		. Nut, tubular, 4-40 x 1/2
-		04N45635A01	2		. Washer, internal lock #4
-		40-F7866G01	1	D1(A)	SWITCH ASSEMBLY - CARD/PAGE
-36	S3	40CF7363F04	1		. Switch, rocker
					/ attaching hardware /
-		02A46698D01	2		. Nut, tubular, 4-40 x 1/2
-		04N45635A01	2		. Washer, internal lock #4
-		40-F7864G01	1	F2(A), F4(A)	SWITCH ASSEMBLY - FEED CONTROL
-37	S2	40CF7363F02	1		. Switch, rocker
					/ attaching hardware /
-		02A46698D01	2		. Nut, tubular, 4-40 x 1/2
-		04N45635A01	2		. Washer, internal lock #4
-38		58CF7859G01	1	I9	ADAPTER ASSEMBLY, TTY
-		15-F7801G01	1	-	HOUSING ASSEMBLY
-39		15DF7378H01	1		. Housing, Hood
-39		27DF7379H01	1		. Housing, Base
-40		64-F7802G01	1		ASSEMBLY, REAR PLATE
					/ attaching hardware /
-41		03AF9001E05	4		. Screw, phillips, pan head, 4-40 x 5/8
-42		02N45571E01	4		. Nut, speed, 4-40
					---*---
-	XF1	09N45280C01	1		. Holder, fuse
-	F1	65N46939A16	1		. Fuse, 3AG, 3A
-		30N46990A08	1		. Cord, ac
-43		40-F7861G01	1	C0	STANDBY SWITCH KIT
43-	S5	40N45224C01	1		. Switch, toggle, DPDT, Cutler Hammer 8363K6

Figure Index Number	Reference Designation	Motorola Part Number	Qty	Usable On Code	Description
					/ attaching hardware /
43 -		04N46963A30	1		. Washer, locking ring
-		30-F7899G01	1	-	HARNESS ASSEMBLY, SENSOR CABLE
					/ attaching hardware /
-44		03AF9001G04	1		Screw, phillips, pan head, 6-32 x 1/4
-45		04N45635A02	1		Washer, flat #6
-46		42N45537E01	1		Clamp, cable
-47		03AF9001E08	1		Screw, phillips, 4-40 x 1/2
-48		04N45854B03	1		Washer, internal lock #4
					---*---
-49	P9	28N46907A64	1		. Connector, 30-pin, Cinch
-50	P14	28N46907A49	1		. Connector, 3-pin, Elco
-51	P13	28N46907A68	1		. Connector, 14-pin, Elco
-		30-F7885G01	1		HARNESS ASSEMBLY, AC CABLE
					/ attaching hardware /
-52		42N45537E01	1		Clamp, cable
					---*---
-53	P1	28N46907A54	1		. Connector, 6-pin, Amplok
-54	J4	28N46907A58	1		. Connector, 4-pin, Amplok
-		30-F7883G01	1		HARNESS ASSEMBLY, DC CABLE
					/ attaching hardware /
-55		42N45537E01	1		Clamp, cable
					---*---
-56	J5	28N46907A60	1		. Connector, 9-pin in line, Amplok
-57	P2	28N46907A54	1		. Connector, 6-pin, Amplok
-58	P3	28N46907A55	1		. Connector, 9-pin, Amplok
-59	P7	28N46907A56	1		. Connector, 12-pin, Amplok
-60	J6	28N46907A62	1		. Connector, 12-pin in line, Amplok
-61	P10	28N46907A64	1		. Connector, 30-pin contact
-62	J15	28N46907A65	1		. Connector, 25-pin contact
-63	A1	01-F7804G01	1	-	ASSEMBLY, CARD CAGE
					/ attaching hardware /
-64		03AF9001J07	4		Screw, phillips, pan head, 10-24 x 7/16
-65		04S7658	4		Washer, internal lock #10
					---*---
-66	P5	28N46907A55	1		. Connector, 9-pin, Amplok
-67		01-F7807G01	1		ASSEMBLY, DRIVE MECHANISM
					/ attaching hardware /
-68		03N46997A19	4		Screw, socket head, 10-24 x 1/2
-69		04N47976A04	4		Washer, flat #10
-70		15DF7361F01	1	-	HOUSING, AIR DUCT
-		67-F7837G01	1	A1, A2	KIT, AUDIBLE ALARM
-71	DS4	80N47958A02			. Alarm, audible
					/ attaching hardware /
-72		29N46926A29	1		. Lug, retaining ring
					---*---
-73	S4	40N45224C01	1		. Switch, toggle, DPDT, Cutler Hammer 8363K6
					/ attaching hardware /
-74		04N46963A30	1		. Washer, locking ring
-75	PS1	01-F7893G01	1	-	ASSEMBLY, POWER SUPPLY
					/ attaching hardware /
-76		03AF9001J05	2		Screw, phillips, pan head, 10-24 x 5/16
43 -77		03AF9001J07	1		Screw, phillips, pan head, 10-24 x 7/17

Figure Index Number	Reference Designation	Motorola Part Number	Qty	Usable On Code	Description
43-78		47BF7309F01	1		Post, support
-79		04S7658	3		Washer, internal lock #10
-80		64DF7299F01	1	-	PLATE, BASE
					/ attaching hardware /
-81		03AF9001J12	4		Screw, phillips, pan head, 10-24 x 3/4
-82		75N47919A05	4		Bumper, rubber
-83		05N46974A24	4		Eyelet, 0.215 dia. x 0.375
-84		47BF7309F01	1		Post, support
-85		04S129582	1		Washer, flat #10 5/16 od
-86	TB1	31N46920A54	1	-	STRIP, BARRIER, 3-TERMINAL
					/ attaching hardware /
-87		11N46921A25	1		Strip, marker
43-88		03AF9001J10	4		Screw, phillips, pan head, 10-24 x 5/8
Ref		01-F7807G01			DRIVE MECHANISM ASSEMBLY (See Figure 43-67)
44-1	A2	01-F7810G01	1	-	ASSEMBLY, L/T SENSOR
					/ attaching hardware /
-2		03AF9001E05	2		Screw, phillips, pan head, 4-40 x 5/16
-3		04N45854B03	2		Washer, internal lock #4
-4		42N46955A07	1	F2, F4	BELT, DRIVE TIMING
-5		47BF7846C01	1	F2, F4	SHAFT, FEED ROLL
					/ attaching hardware /
-6		43N47955A04	2		Bearing, for 0.25 shaft
-7		04N46963A31	1		Washer, nylon, 0.032 thick
-8		01CF7831G01	1	F2, F4	ASSEMBLY, FEED ROLL
					/ attaching hardware /
-9		03N47984A10	2		Screw, knurled set, 8-32 x 3/16
-10		49N47910B02	1	F2, F4	DRIVE PULLEY, FEED ROLLER, 28T
					/ attaching hardware /
-11		03N47984A10	1		Screw, knurled set, 8-32 x 3/16
-12		49N47910B03	1	F2, F4	DRIVE PULLEY, HOPPER, 14T
					/ attaching hardware /
-13		03N47984A10	1		Screw, knurled set, 8-32 x 3/16
-		01-F7830G01	1	F2, F4	ASSEMBLY, CLUTCH SHAFT
					/ attaching hardware /
-14		43N47955A04			Bearing, for 0.25 shaft
					---*---
-15		47BF7847C01	1		. Shaft, feed clutch
-16		45CF7888C01	1		. Cam, skip feed
					/ attaching hardware /
-17		03N47984A10	1		. Screw, knurled set, 8-32 x 3/16
					---*---
-18		44CF7885C01	1		. Gear, feed drive
-19	CR1	48N45715D04	1		. Diode, 1N4001
-20	L1	49N47911B02	1		. Clutch, solenoid
					/ attaching hardware /
-21		42BF7889C01	2		. Retainer, clutch solenoid
-22		03N46925A36	2		. Screw, phillips, thread forming, 6-32 x 1/4
-23		22N46951A18	1		. Pin, roll, 1/16 dia. x 3/8
44-24		03AF9001G04	3		. Screw, phillips, pan head, 6-32 x 1/4

Figure Index Number	Reference Designation	Motorola Part Number	Qty	Usable On Code	Description
44-25		07-F7835G01	1	F4	BRACKET ASSEMBLY, TRIP
					/ attaching hardware /
-26		03AF9002J14	1		Screw, phillips, pan head, 10-32 x
-27		04N47976A04	1		Washer, flat #10
-28		41BF7317F01	1		Spring, torsion
-29		43BF7318F01	1		Bushing, shoulder
-30		07-F7775G02	1	F4	BRACKET ASSEMBLY, IDLER-SKIP
					/ attaching hardware /
-31		03N46997A07	2		Screw, socket head, 10-32 x 1/2
-32		04S7658	2		Washer, internal lock #10
-33		04N47997A07	2		Washer, flat #10
-34		42N46955A06	1	F4	BELT, DRIVE, 3M272
-35		47CF6845C02	1		SHAFT
					/ attaching hardware /
-36		43N47955A04	2		Bearing, for 0.25 shaft
-37		49N47911B01	1		Clutch, overdrive shaft
-38		49CF7531F01	1	F4	CLUTCH, EJECT FEED
					/ attaching hardware /
-39		03N47984A10	1		Screw, knurled set, 8-32 x 3/16
-40		42N46955A06	1	F4	BELT, DRIVE, 3M272 (Ref. Figure 45-18)
-41		49N47910B01	1	F4	PULLEY, 2.48 OD
					/ attaching hardware /
-42		03N47984A10	1		Screw, knurled set, 8-32 x 3/16
-43		01-F7816G01	1	-	ASSEMBLY, IDLER ROLLER
					/ attaching hardware /
-44		03N46925A86	2		Screw, socket head, 8-32 x 3/8
-45		04N45635A03	2		Washer, flat #8
-46	S6	40N46916A62	1	A1, A2	SWITCH, LIGHT FORCE, SPDT
					/ attaching hardware /
-47		07BF7525F01	1		Bracket, switch
-48		07BF7525F02	1		Bracket, switch
-49		03AF9001C10	2		Screw, phillips, pan head, 2-56 x 5/8
-50		04N45854B01	2		Washer, lock #2
-51		02AF9021C01	2		Nut, hex, 2-56 x 3/16
-52		03AF9001E03	4		Screw, phillips, pan head, 4-40 x 3/16
-53	S7	40N46916A61	1	F2, F4	SWITCH, PUSHBUTTON
					/ attaching hardware /
-54		02AF9024C01	2		Nut, hex, 3/8-24 x 9/16
-55		42N46955A06	1	SA	BELT, DRIVE 3M272 (Ref. Figure 45-44)
-56		49DF7314F04	1	SA	PULLEY, SHAFT
					/ attaching hardware /
-57		03N47984A10	1		Screw, knurled set, 8-32 x 3/16
-55		42N46955A11	1	SB	BELT, DRIVE, 3M307 (Ref. Figure 45-44)
-56		49DF7314F02	1	SB	PULLEY, SHAFT
					/ attaching hardware /
-57		03N47984A10	1		Screw, knurled set, 8-32 x 3/16
44-58		07-F7775G01	1	-	BRACKET ASSEMBLY, IDLER-MAIN

Figure Index Number	Reference Designation	Motorola Part Number	Qty	Usable On Code	Description
					/ attaching hardware /
44-59		03N46997A07	2		Screw, socket head, 10-32 x 1/2
-60		04S7658	2		Washer, internal lock #10
-61		04N47976A04	2		Washer, flat #10
-62		42N46955A08	1	–	BELT, DRIVE, 3M412 (Ref. Figure 45-16)
-63		49N47910B05	1	–	PULLEY, MAIN SHAFT
					/ attaching hardware /
-64		03N47984A10	1		Screw, knurled set, 8-32 x 3/16
-65		49N47910B06	1	–	PULLEY, EJECT, MAIN SHAFT
					/ attaching hardware /
-66		03N47984A10	1		Screw, knurled set, 8-32 x 3/16
-		01-F7817G01	1	–	ASSEMBLY, MAIN SHAFT
					/ attaching hardware /
-67		43N47955A04	2		Bearing, for 0.25 shaft
					---*--
-68		47CF7845C01	1		. Shaft, main
-69		44BF7244F01	1		. Gear, main drive
					/ attaching hardware /
-70		22N46951A23	1		. Pin, roll, 1/16 dia. x 5/8
-71		07CF7874C01	1	–	BRACKET, ANTI-STATIC
-72		55CF7779B01	1	–	LATCH, RECEIVER, CARD
					/ attaching hardware /
-73		03N47932A05	2		Screw, phillips, flat head, 8-32 x 5/16
-74	J7	28N46907A63	1	–	CONNECTOR, 12-PIN, AMPLOK
					/ attaching hardware /
-75		07BF7735B01	1		Bracket, connector
-76		03AF9001E04	4		Screw, phillips, pan head, 4-40 x 1/4
-77		04N45854B03	4		Washer, internal lock #4
-		01-F7811G01	1	–	ASSEMBLY, DRIVE FRAME
					/ attaching hardware /
-78		03AF9001G05	4		Screw, phillips, pan head, 6-32 x 5/16
-79		04N45635A02	4		Washer, flat #6
-80		42N45537E01	2		Clamp, cable
-81		46BF7334F01	1		Stud, latching
-82		04N46963A35	1		Washer, split, flat #8
-83		04N45635A03	1		Washer, flat #8
-84		04N45854B06	1		Washer, internal lock #8
-85		02AF9021H01	1		Nut, hex, 8-32 x 11/32
-86		07BF7769B01	1		Bracket, housing, drive end
-87		02N45223B01	1		Nut, u-type
-88		04S7650	2		Washer, internal lock #6
					---*---
44-89		07DF7842C01	1		. Frame, drive (Ref. Figure 45-60)
Ref.		01-F7807G01			DRIVE MECHANISM ASSEMBLY (Ref. Figure 43-67)
45-1	A4	01-F7806G01	1	–	ASSEMBLY, SENSOR LAMP
-2		65N46952A45	12	–	. Lamp, bi-pin base, 6V 200mA, Chicago Mini. CM7-349
45-		01-F7812G01	1	–	FRAME ASSEMBLY, DRIVE ROLLER

Figure Index Number	Reference Designation	Motorola Part Number	Qty	Usable On Code	Description
					/ attaching hardware /
45-3		03N45042B02	4		Screw, socket head, 10-32 x 5/8
-4		04S7658	4		Washer, internal lock #10
-5		43N45537E01	1		Clamp, cable
-6		04N45635A04	4		Washer, flat #10
					---*---
-7		07DF7843C01	1		. Frame, drive roller
-8		43N47955A04	4		. Bearing, for 0.25 shaft
-9		03N45478B04	2		. Screw, set, 10-32 x 1/2
-10		01BF7815G01	2		. Assembly, drive roller
-11		43N46927A61	2		. Spacer, 1/4 ID x 0.337 1/2 OD
-12		01-F7814G01	2		. Assembly, clutch pulley
					/ attaching hardware /
-13		42N46986A08	2		. Ring, grip, ext-truarc
-14		04S131332	2		. Washer, cadmium steel, 0.264 thick
-15		04N46963A31	4		. Washer, nylon, 0.032 thick
-16		42N46955A08	1	-	BELT, DRIVE, 3M412 (Ref. Figure 44-62)
-17		01-F7814G01	1	F4	ASSEMBLY, CLUTCH PULLEY
-18		42N46955A06	1	F4	BELT, DRIVE 3M272 (Ref. Figure 44-40)
-19		45-F7776G01	1	F4	ARM ASSEMBLY, IDLER-EJECT
					/ attaching hardware /
-20		03N46997A03	2		Screw, socket head, 10-32 x 1/2
-21		04S7658	2		Washer, internal lock #10
-22		04N47976A04	2		Washer, flat #10
-		01-F7808G01	1	–	ASSEMBLY, SENSOR HEAD
					/ attaching hardware /
-23		03N46925A27	2		Screw, phillips, thread forming, 4-40 x 3/8
-24	P12	28N46907A51	1		Connector, 3-pin, Elco
-25		03N46997A11	2		Screw, socket head, 4-40 x 1/4
					---*--
-26		59C7510F01	1		. Head, sensing
-27		01-F7809G01	1		. Assembly, data sensor
					/ attaching hardware /
-28		03N47932A01	3		. Screw, phillips, flat head, 2-56 x 1/4
					---*---
-29		41CF7807C01	1		. Spring, hold down
					/ attaching hardware /
-30		03AF9001C03	3		. Screw, phillips, pan head, 2-56 x 3/16
-31		04N45854B01	3		. Washer, internal lock #2
-32		04N45635A06	3		. Washer, flat #2
-33		07-F7777G01	1	–	BRACKET, ASSEMBLY, IDLER-MOTOR
					/ attaching hardware /
-34		03-F7778G01	1		Assembly, shoulder screw
-35		03AF9002J06	1		Screw, phillips, pan head, 10-32 x 3/8
-36		04N45635A04	2		Washer, flat #10
-		67-F7838G01	1	SA	KIT, DRIVE MOTOR - 7 CHARACTERS/SECOND
-		59-F7779G01	1		. Assembly, motor
					/ attaching hardware /
-37		03AF9001J05			. Screw, phillips, 10-24 x 3/8
					---*---
-38	B1	59N47921A04	1		. . Motor, 115 Vac, 60 Hz, 17 rpm
-39	P8	28N46907A52	1		. . Connector, 3-pin, Amplok
-40		07CF7846G01	1		. Bracket assembly, motor mounting
					/ attaching hardware /
45-41		03AF9002J06	4		. Screw, phillips, pan head, 10-32 x 3/8

Figure Index Number	Reference Designation	Motorola Part Number	Qty	Usable On Code	Description
45-42		04S7658	4		. Washer, internal lock #10
-43		04N45635A04	4		. Washer, flat #10
					---*---
-44		42N46955A06	1		. Belt, drive, 3M272 (Ref. Figure 44-55)
-45		49DF7314F03	1		. Pulley, motor
					/ attaching hardware /
-46		03N47984A10	1		. Screw, knurled set, 8-32 x 3/16
					---*---
-47		58CF7332F01	1		. Adapter, motor shaft
					/ attaching hardware /
-48		03N47984A09	1		. Screw, set, 10-32 x 3/16
					---*---
Ref.		49DF7314F04	1		. Pulley, shaft (Ref. Figure 44-56)
					/ attaching hardware /
Ref.		03N47984A10	1		. Screw, knurled set, 8-32 x 3/16 (Ref. Figure 44-57)
-		67-F7838G02	1	SB	KIT, DRIVE MOTOR - 70 CHARACTERS/SECOND
-		59-F7779G02	1		. Assembly, motor
					/ attaching hardware /
-37		03AF9001J05	4		. Screw, phillips, 10-24 x 3/8
					---*--
-38	B1	59N47921A05	1		. . Motor, 115 Vac, 60 Hz, 96 rpm
-39	P8	28N46907A52	1		. . Connector, 3-pin, Amplok
-40		07CF7846G01	1		. Bracket assembly, motor mounting
					/ attaching hardware /
-41		03AF9002J06	4		. Screw, phillips, pan head, 10-32 x 3/8
-42		04S7658	4		. Washer, internal lock #10
-43		04N45635A04	4		. Washer, flat #10
					---*---
-44		42N46955A11	1		. Belt, drive 3M307 (Ref. Figure 44-55)
-45		49DF7314F01	1		. Pulley, motor
					/ attaching hardware /
-46		03N47984A10	1		. Screw, knurled set, 8-32 x 3/16
					---*---
Ref.		49DF7314F02	1		. Pulley, shaft (Ref. Figure 44-56)
					/ attaching hardware /
Ref.		03N47984A10	1		. Screw, knurled set, 8-32 x 3/16 (Ref. Figure 44-57)
-49		07-F7775G03	1	F2, F4	BRACKET ASSEMBLY, IDLER-FEED
					/ attaching hardware /
-50		03N46997A07	2		Screw, socket head, 10-32 x 1/2
-51		04S7658	2		Washer, internal lock #10
-52		04N47976A04	2		Washer, flat #10
-53		07BF7303F01	1	-	BRACKET, LATCH
					/ attaching hardware /
-54		03N46997A11	2		Screw, socket head, 4-40 x 1/4
-55		07BF7770B01	1	-	BRACKET, HOUSING, HEAT SINK SIDE
					/ attaching hardware /
-56		02N45223B01	1		Nut, u-type, 6-32
-57		03AF9001G05	2		Screw, phillips, pan head, 6-32 x 5/16
-58		04S7650	2		Washer, internal lock #6
-59		04N45635A02	2		Washer, flat #6
45-60		01-F7811G01	1	-	ASSEMBLY, DRIVE FRAME

Figure Index Number	Reference Designation	Motorola Part Number	Qty	Usable On Code	Description
Ref.	PS1	01-F7893G01			POWER SUPPLY ASSEMBLY (See Figure 43-75)
46-1	A1	01-F7896G01	1	–	ASSEMBLY, LAMP SUPPLY
					/ attaching hardware /
-2		03N46925A25	4		Screw, phillips, thread forming, 4-40 x 1/4
-3		04B47728C01	4		Washer, flat #4
					---*---
		42N45752E01	2		. Clip, fuse
	F1	65N46939A16	1		. Fuse, 3A, 3AG
	R3	17N46913B90	1		. Resistor, wirewound, 4.7, 2W, 10%
	R2	06S126C37	1		. Resistor, 330, 1W, 10%
	R10, 11	06S125C25	2		. Resistor, 100, 1/2W, 10%
	R8, 9	06S125C03	2		. Resistor, 12, 1/2W, 10%
	R12	06S125C19	1		. Resistor, 56, 1/2W, 10%
	R5	06S125C49	1		. Resistor, 1K, 1/2W, 10%
	R1	06S125C59	1		. Resistor, 2.7K, 1/2W, 10%
	R6	06S125C61	1		. Resistor, 3.3K, 1/2W, 10%
	R7	06S125C64	1		. Resistor, 4.7K, 1/2W, 10%
	R4	18N45786A06	1		. Potentiometer, wirewound, 1K, 20%
	C3, 4	23N46914A11	2		. Capacitor, 50 μF, 50V
	C2	23N46914A41	1		. Capacitor, 2300 μF, 50V
	C1	23N46914A40	1		. Capacitor, 2200 μF, 25V
	CR1	48N46917A18	1		. Rectifier, bridge, type MDA-970-2
	VR1	48N46938A89	1		. Diode, zener, 1N5242, 12V
	VR2	48N46938A90	1		. Diode, zener, 1N5251, 22V
	CR2	48N45715D04	1		. Diode, 1N4001
	Q2	48N47908B07	1		. Transistor, 2N2907
	Q1	48N47908B03	1		. Transistor, 2N4918
	Q3, 4	48N46929A26	2		. Transistor, 2N4403
-4	A2	01-F7895G01	1	–	ASSEMBLY, IC SUPPLY
					/ attaching hardware /
		03N46925A25	4		Screw, phillips, thread forming, 4-40 x 1/4
		04B47728C01	4		Washer, flat #4
					---*---
	R1	17N46933A58	1		. Resistor, wirewound, 0.33, 2W, 10%
	R6	06S125C09	1		. Resistor, 22, 1/2W, 10%
	R9	06S125C11	1		. Resistor, 27, 1/2W, 10%
	R8, 13	06S125C19	2		. Resistor, 56, 1/2W, 10%
	R10, 12	06S125C25	2		. Resistor, 100, 1/2W, 10%
	R5	06N47930A47	1		. Resistor, 120, 1/2W, 10%
	R3	06S125C43	1		. Resistor, 560, 1/2W, 10%
	R11	06S125C49	1		. Resistor, 1K, 1/2W, 10%
	R2	06S125C55	1		. Resistor, 1.8K, 1/2W, 10%
	R4	06S125C57	1		. Resistor, 2.2K, 1/2W, 10%
	R7	18N46935A93	1		. Potentiometer, wirewound, 100, 2W, 20%
	C2, 3	08D82905G01	2		. Capacitor, 0.01 μF, 50V
	C1	23N46914A40	1		. Capacitor, 2200 μF, 25V
	C4	23N45223A15	1		. Capacitor, 15 μF, 35V
	CR1	48N46917A18	1		. Rectifier, bridge, type MDA-970-2
	SCR1	48N46917A19	1		. S.C.R., 2N4441
	CR2	48N46967A11	1		. Diode, MR2361
	VR1, 2	48N46938A76	2		. Diode, zener, 1N5221, 2.4V
	VR3	48N46938A92	1		. Diode, zener, 1N5234, 6.2V
	Q2, 3	48N45857B01	2		. Transistor, 2N2218
	Q1, 4	48N47908B07	2		. Transistor, 2N2907
46-5	A3	01-F7894G01	1	–	ASSEMBLY, COMPONENT POWER SUPPLY
					/ attaching hardware /
		03N46925A25	4		Screw, phillips, thread forming, 4-40 x 1/4
		04B47728C01	4		Washer, flat #4
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Figure Index Number	Reference Designation	Motorola Part Number	Qty	Usable On Code	Description
	R6	17N46933A58	1		. Resistor, wirewound, 0.33, 2W, 10%
	R7	06S125C33	1		. Resistor, 220, 1/2W, 10%
	R5	06S125C25	1		. Resistor, 100, 1/2W, 10%
	R1, 2	06S125C43	2		. Resistor, 560, 1/2W, 10%
	R4	06S125C49	1		. Resistor, 1K, 1/2W, 10%
	R3	06S125C61	1		. Resistor, 3.3K, 1/2W, 10%
	C7	23N45223A15	1		. Capacitor, 15 μF, 35V
	C4, 5	23D82601A06	2		. Capacitor, 60 μF, 50V
	C6	08D82905G07	1		. Capacitor, 0.1 μF, 50V
	C1	23N46914A40	1		. Capacitor, 2200 μF, 25V
	C3	23N46914A44	1		. Capacitor, 4000 μF, 25V
	CR1	48N46917A18	1		. Rectifier, bridge, type MDA-970-2
	VR1	48N46938A87	1		. Diode, zener, 1N5243, 13V
	VR2	48N46938A96	1		. Diode, zener, 1N5248, 16V
	Q1	48N45857B01	1		. Transistor, 2N2218
	SCR1	48N46917A19	1		. S.C.R., 2N4441
46-6	T1	25CF7775B01	1	–	TRANSFORMER
					/ attaching hardware /
		03N46925A66	4		Screw, flat head, 8-32 x 1-1/2
		04N45854B06	8		Washer, internal lock #8
		02N45468A03	4		Nut, hex, 8-32
-7	T2	25CF7776B01	1	–	TRANSFORMER
					/ attaching hardware /
		03N46925A62	4		Screw, flat head, 8-32 x 2-1/4
		04N45854B06	8		Washer, internal lock #8
		02N45468A03	4		Nut, hex, 8-32
-8	XF1, 2, 3	09N45280C01	3	–	HOLDER, FUSE
-9A	F1, 2	65N46939A16	2	–	FUSE, 3AG, 3A
-9B	F3	65N46939A19	1	–	FUSE, 3AG, 5A
-10	XK1, 2, 3	09N45944D02	3	–	SOCKET, RELAY
	CR1, 2	48N45715D04	2	–	DIODE, 1N4001
		67-F7860G01	1	CO	RELAY KIT
-11A	K1	80BF7782B01	1		. Relay, 117 Vac, 4 PDT
-11B	K2, 3	80N46909A65	2		. Relay, 12 Vdc, 4PDT
-11	K2	28BF7862G01	1	C1, C2	PLUG, JUMPER (K1 and K3 not used)
-12A	J1, 2	28N46907A59	2	–	CONNECTOR, 6-PIN, AMPLOK
-12B	J3	28N46907A61	1	–	CONNECTOR, 9-PIN, AMPLOK
		01-F7909G01	1	-	ASSEMBLY, COOLER
					/ attaching hardware /
-13		03N46925A38	4		Screw, phillips, thread forming, 6-32 x 3/8
-14		04N45854B05	4		Washer, internal lock #6
-15		04N45635A02	4		Washer, flat #6
					---*---
-16		01CF512G01	1		. Assembly, heat sink
					/ attaching hardware/
-17		02AF9021G02	4		. Nut, hex, 6-32
-18		04S7650	4		. Washer, internal lock #6
-19		03BF7789E01	4		. Screw, shoulder, 6-32 x 9/16
-20		04N45635A02	4		. Washer, flat #6
-21		04N45854B05	4		. Washer, internal lock #6
-22		02AF9021G02	4		. Nut, hex, 6-32 x 1/4
					---*---
46-23	B1	59N46921A06	1		. . Motor, blower, 117 Vac, 60 Hz, 14W, Rotron SP2A2

Figure Index Number	Reference Designation	Motorola Part Number	Qty	Usable On Code	Desc
46-24	Q1	48N45248A01	1	–	TRANSISTOR, 2N1544
-24B	Q2,3	48N47909B03	2	–	TRANSISTOR, 2N3715
					/ attaching hardware /
-25		03AF9001G06	2		Screw, phillips, pan head, 6-32 x 3/8
-26		04N45854B05	1		Washer, internal lock #6
		29N45797D01	1		Lug, internal lock #6
46-27		43BF7788B01	2		Spacer, insulator

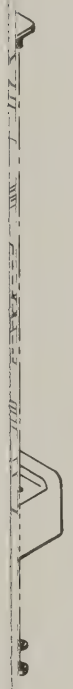
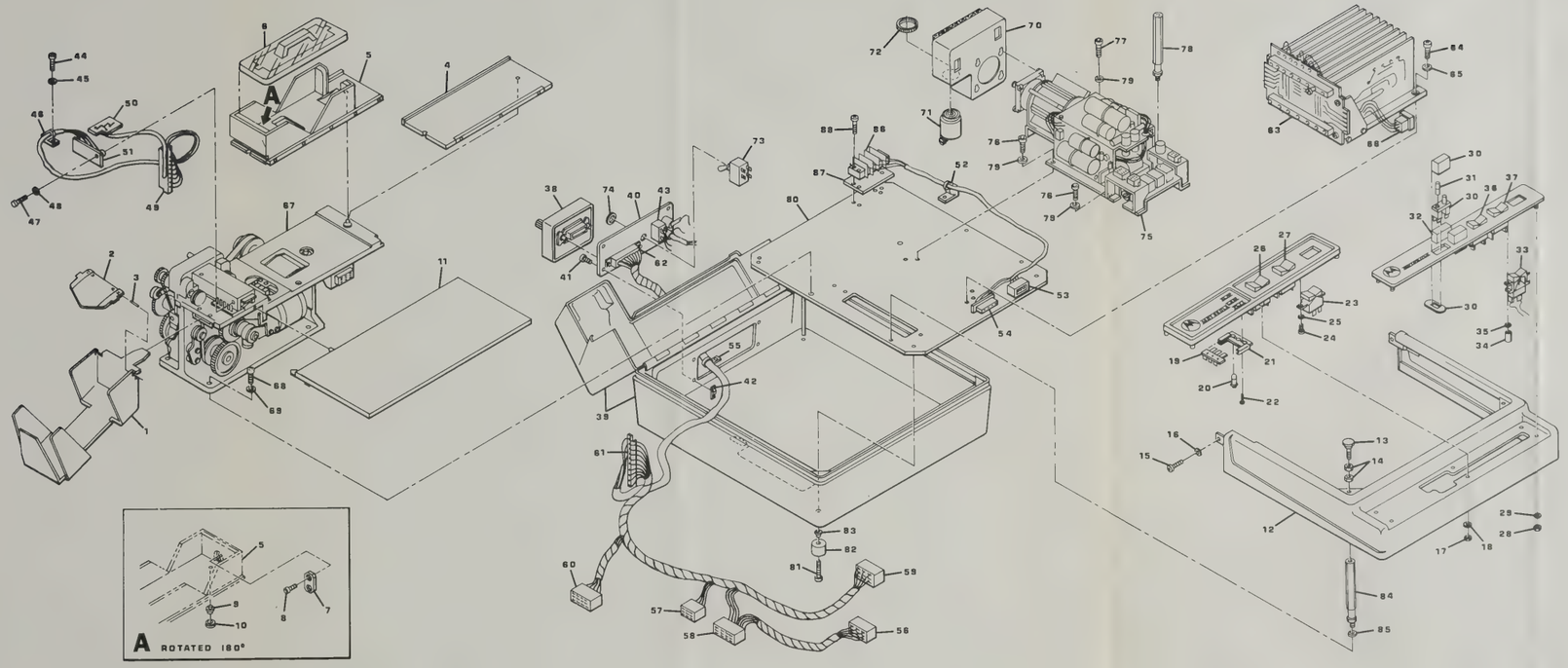
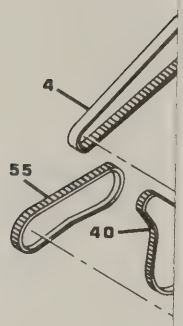


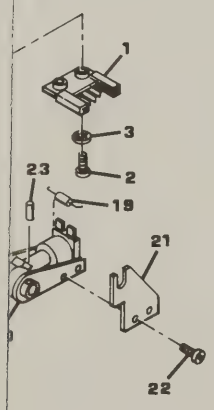
FIGURE 43
MDR EXPLODED VIEW



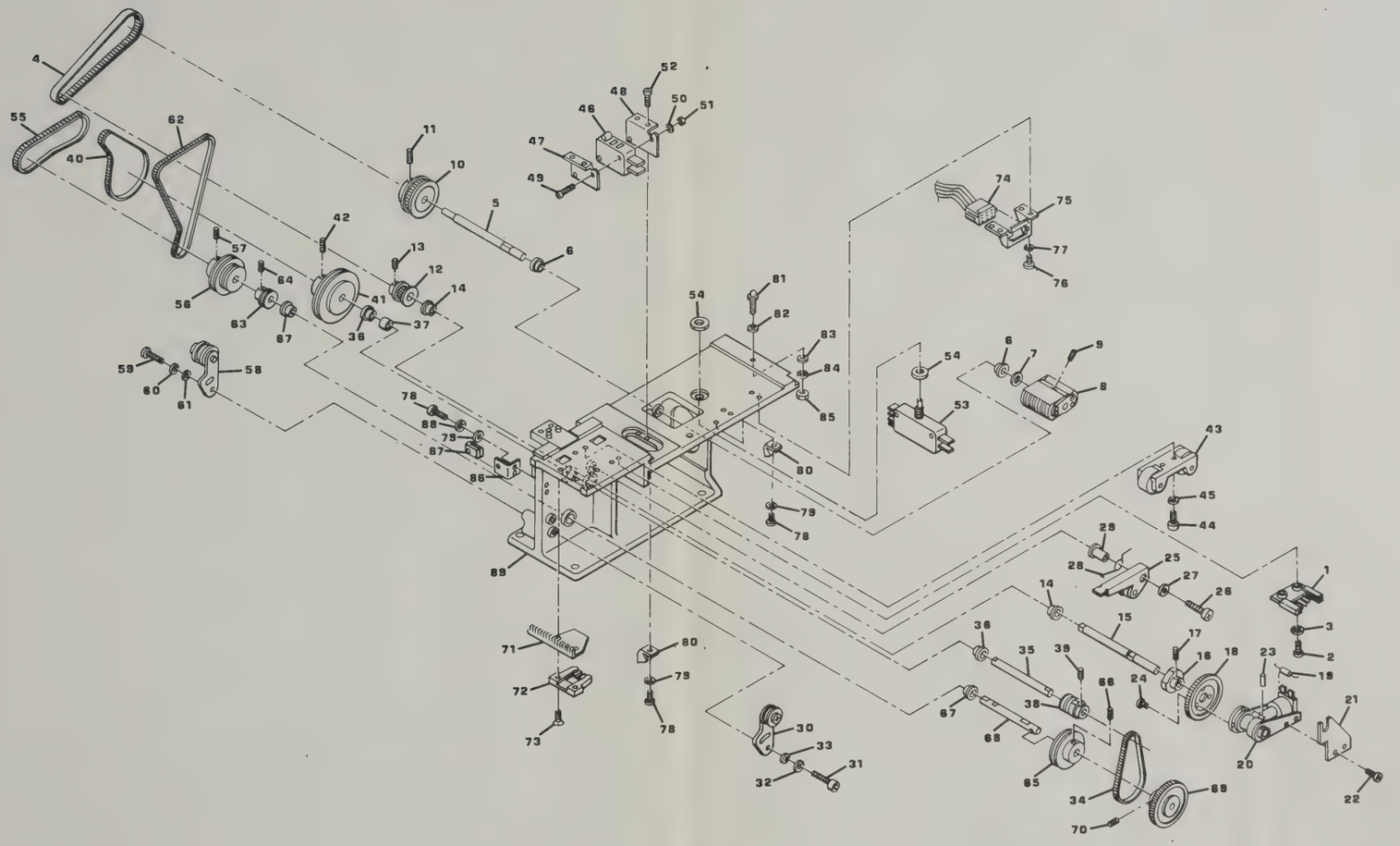
(P/O DWG. NO. 01DF/762H)

FIGURE 43
MDR EXPLODED VIEW





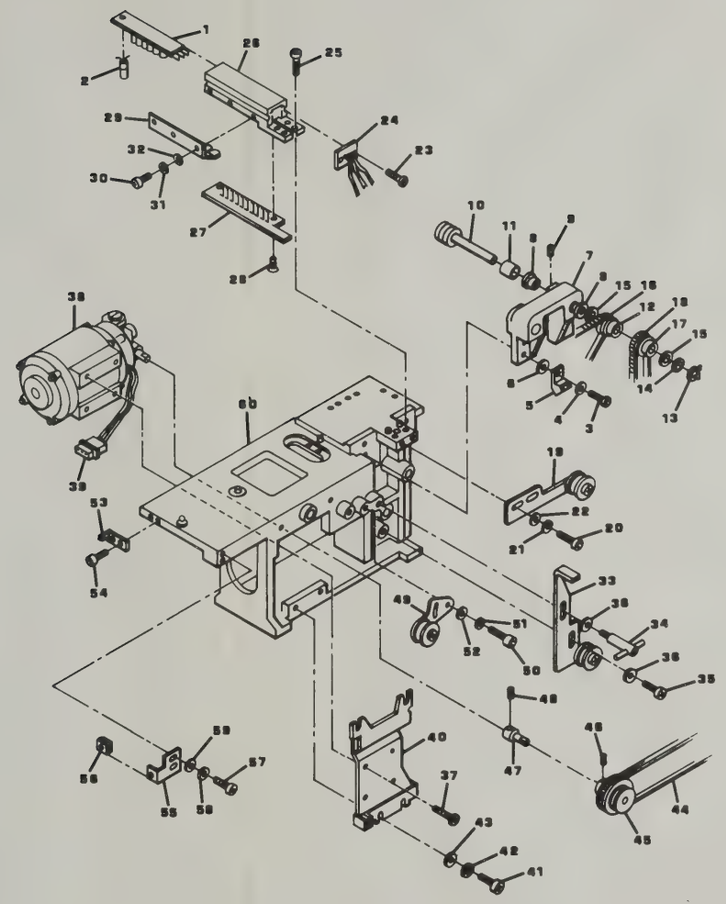
URE 44
R TRANSPORT EXPLODED VIEW (PARTIAL)



(P/O DWG. NO. 01DF7762H)

FIGURE 44
MDR TRANSPORT EXPLODED VIEW (PARTIAL)

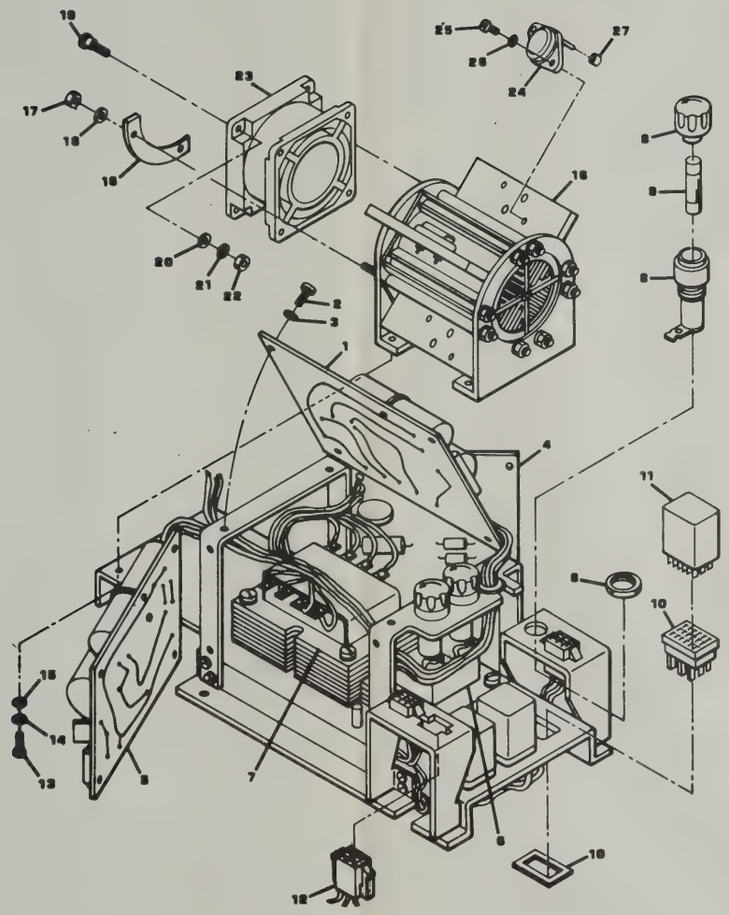
URE 45
R TRANSPORT EXPLODED VIEW (PARTIAL)



(P/O DWG. NO. 01DF7762H)

FIGURE 45
MDR TRANSPORT EXPLODED VIEW (PARTIAL)

FIGURE 46
MDR POWER SUPPLY EXPLODED VIEW



(P/O DWG. NO. 01DF7762H)

FIGURE 46
MDR POWER SUPPLY EXPLODED VIEW

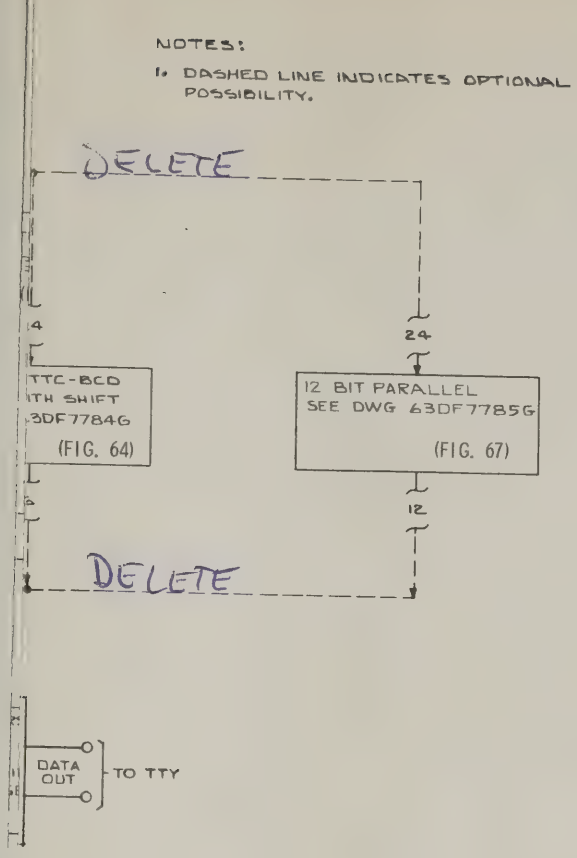


FIGURE 47
MDR SERIAL BLOCK DIAGRAM

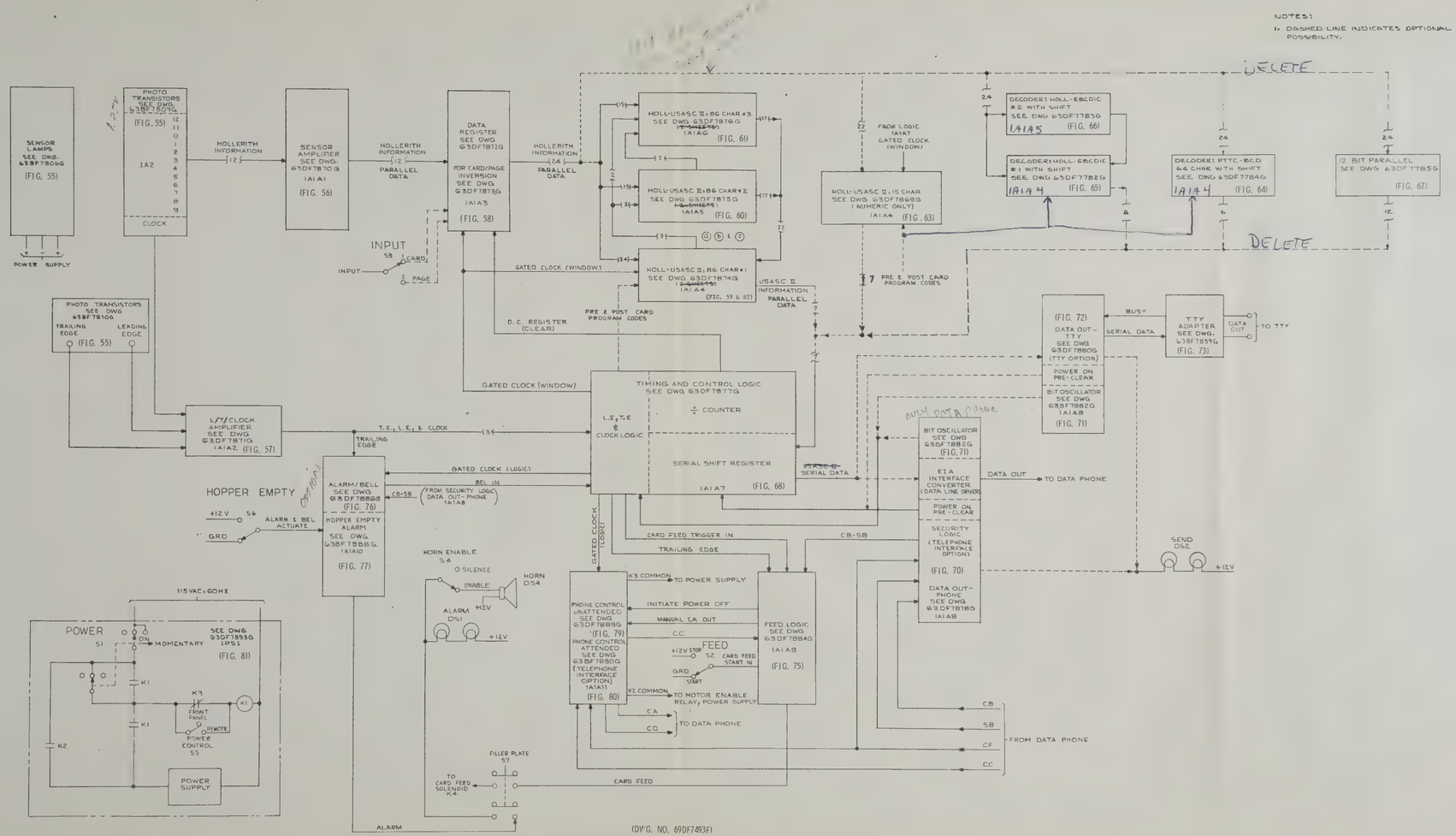


FIGURE 47
MDR SERIAL BLOCK DIAGRAM

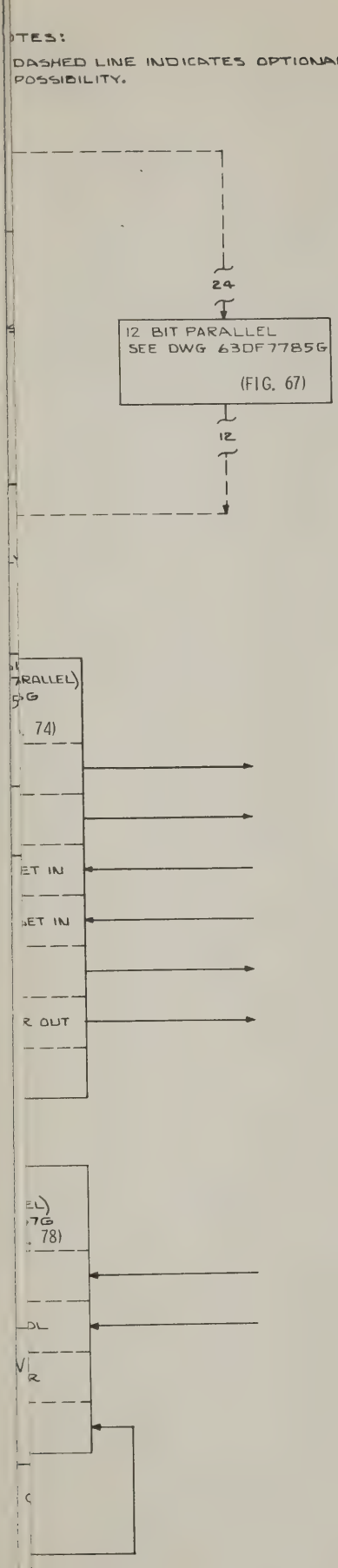


FIGURE 48
MDR PARALLEL BLOCK DIAGRAM

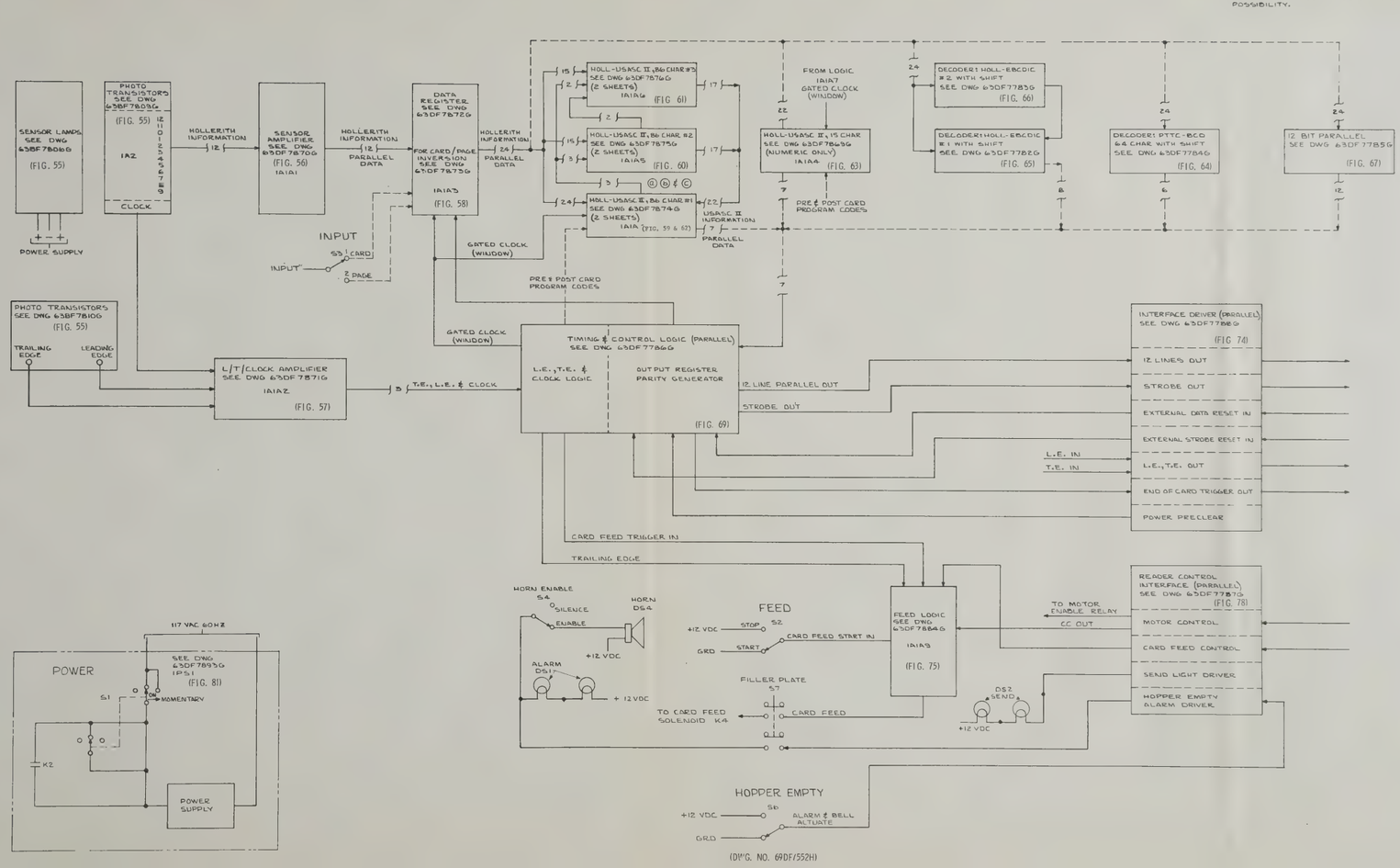

NOTES:
1. DASHED LINE INDICATES OPTIONAL POSSIBILITY.
SENSOR LAMPS SEE DWG 63DF78016 (FIG. 55)
PHOTO TRANSISTORS SEE DWG 63DF78015 (FIG. 55) 1A2
CLOCK
POWER SUPPLY
HOLLERITH INFORMATION
SENSOR AMPLIFIER SEE DWG 63DF78706 (FIG. 56) 1A1A1
DATA REGISTER SEE DWG 63DF78726
FOR CARD/PAGE INVERSION SEE DWG 63DF78736
1A1A3 (FIG. 58)
PARALLEL DATA
INPUT
CARD
PAGE
GATED CLOCK (WINDOW)
PRE & POST CARD PROGRAM CODES
HOLL-USASC II, 86 CHAR #3 SEE DWG 63DF78746 (2 SHEETS) 1A1A6 (FIG. 61)
HOLL-USASC II, 86 CHAR #2 SEE DWG 63DF78756 (2 SHEETS) 1A1A5 (FIG. 60)
HOLL-USASC II, 86 CHAR #1 SEE DWG 63DF78746 (2 SHEETS) 1A1A4 (FIG. 59 & 62)
USASC II INFORMATION
FROM LOGIC 1A1NT GATED CLOCK (WINDOW)
HOLL-USASC II, 15 CHAR SEE DWG 63DF78636 (NUMERIC ONLY) 1A1A4 (FIG. 63)
DECODER: HOLL-EBCDIC #2 WITH SHIFT SEE DWG 63DF77836 (FIG. 66)
DECODER: HOLL-EBCDIC #1 WITH SHIFT SEE DWG 63DF77826 (FIG. 65)
DECODER: PTTC-BCD 64 CHAR WITH SHIFT SEE DWG 63DF77846 (FIG. 64)
12 BIT PARALLEL SEE DWG 63DF77856 (FIG. 67)
PHOTO TRANSISTORS SEE DWG 63BF78106 (FIG. 55)
TRAILING EDGE
LEADING EDGE
L/T/CLOCK AMPLIFIER SEE DWG 63DF78716 1A1A2 (FIG. 57)
T.E., L.E. & CLOCK
TIMING & CONTROL LOGIC (PARALLEL) SEE DWG 63DF77866
L.E., T.E. & CLOCK LOGIC
OUTPUT REGISTER PARITY GENERATOR
(FIG. 69)
12 LINE PARALLEL OUT
STROBE OUT
L.E. IN
T.E. IN
INTERFACE DRIVER (PARALLEL) SEE DWG 63DF77806 (FIG 74)
12 LINES OUT
STROBE OUT
EXTERNAL DATA RESET IN
EXTERNAL STROBE RESET IN
L.E., T.E. OUT
END OF CARD TRIGGER OUT
POWER PRECLEAR
CARD FEED TRIGGER IN
TRAILING EDGE
HORN ENABLE S4
SILENCE
ENABLE
HORN DS4
+12 VDC
ALARM DS1
+ 12 VDC
FEED
+12 VDC
GRD
STOP S2
START
CARD FEED START IN
FILLER PLATE S7
TO CARD FEED SOLENOID K4
CARD FEED
FEED LOGIC SEE DWG 63DF78846 1A1A3 (FIG. 75)
TO MOTOR ENABLE RELAY
CC OUT
DS2 SENSE
+12 VDC
READER CONTROL INTERFACE (PARALLEL) SEE DWG 63DF77876 (FIG. 78)
MOTOR CONTROL
CARD FEED CONTROL
SENSE LIGHT DRIVER
HOPPER EMPTY ALARM DRIVER
HOPPER EMPTY
+12 VDC
GRD
S8
ALARM & BELL ALTUNTE
117 VAC 60HZ
POWER
SEE DWG 63DF78956 1P51 (FIG. 81)
S1
MOMENTARY
K2
POWER SUPPLY
(DWG. NO. 69DF/552H)

FIGURE 48
MDR PARALLEL BLOCK DIAGRAM

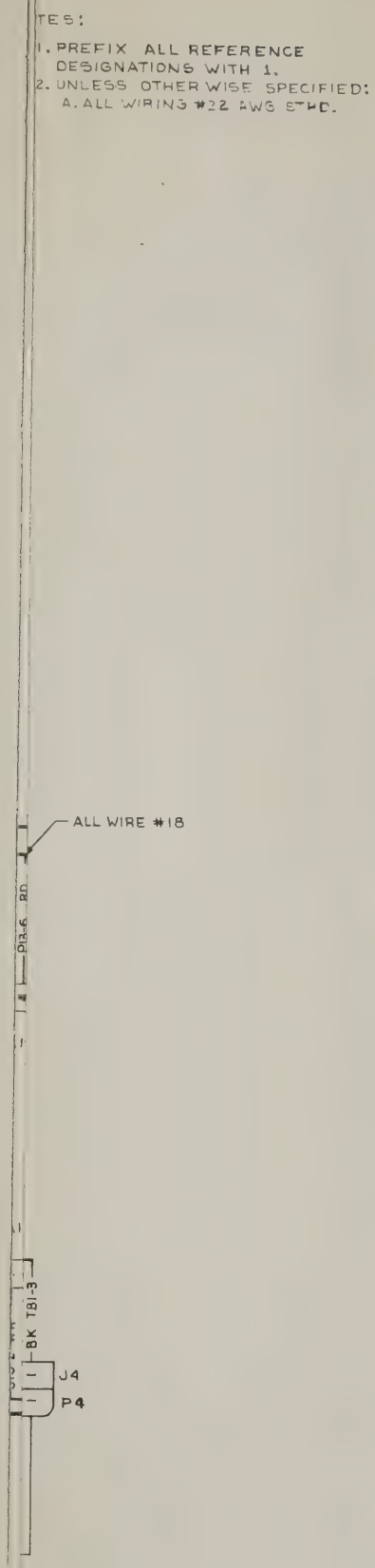
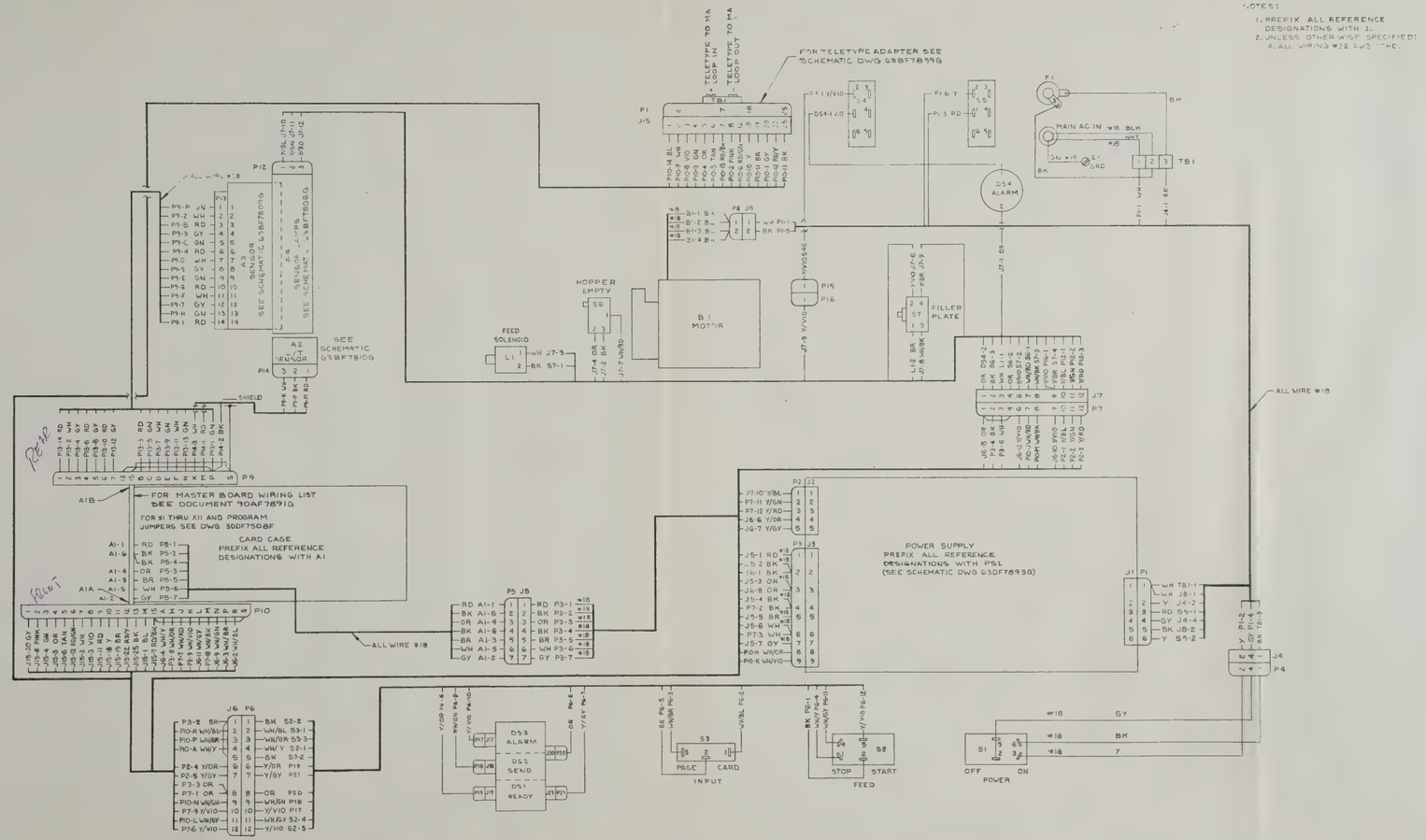


FIGURE 49
MDR SERIAL WIRING DIAGRAM



(DWG. NO. 90DF7509F)

FIGURE 49
MDR SERIAL WIRING DIAGRAM

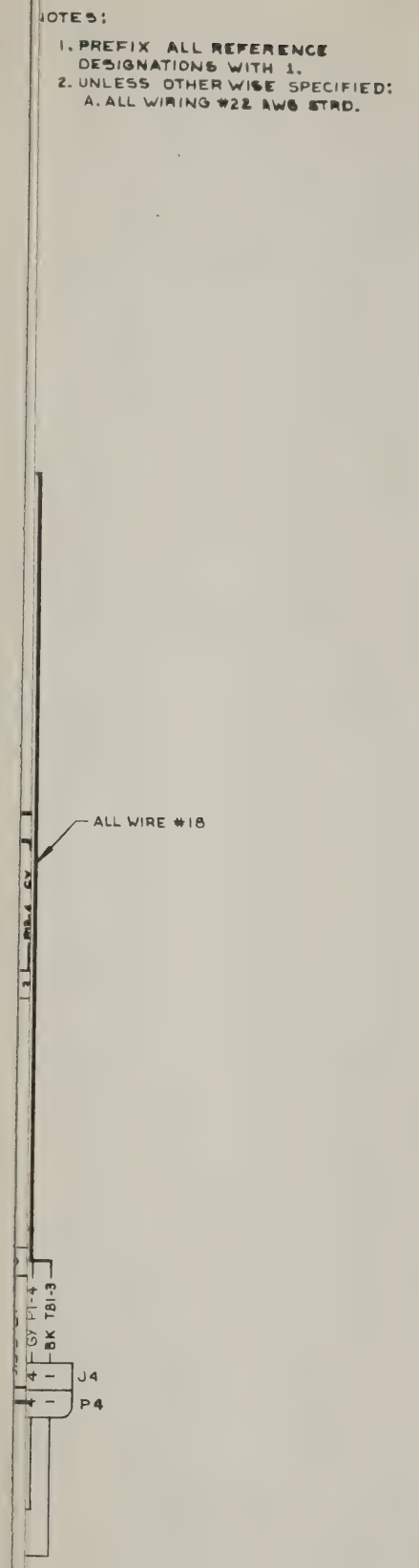
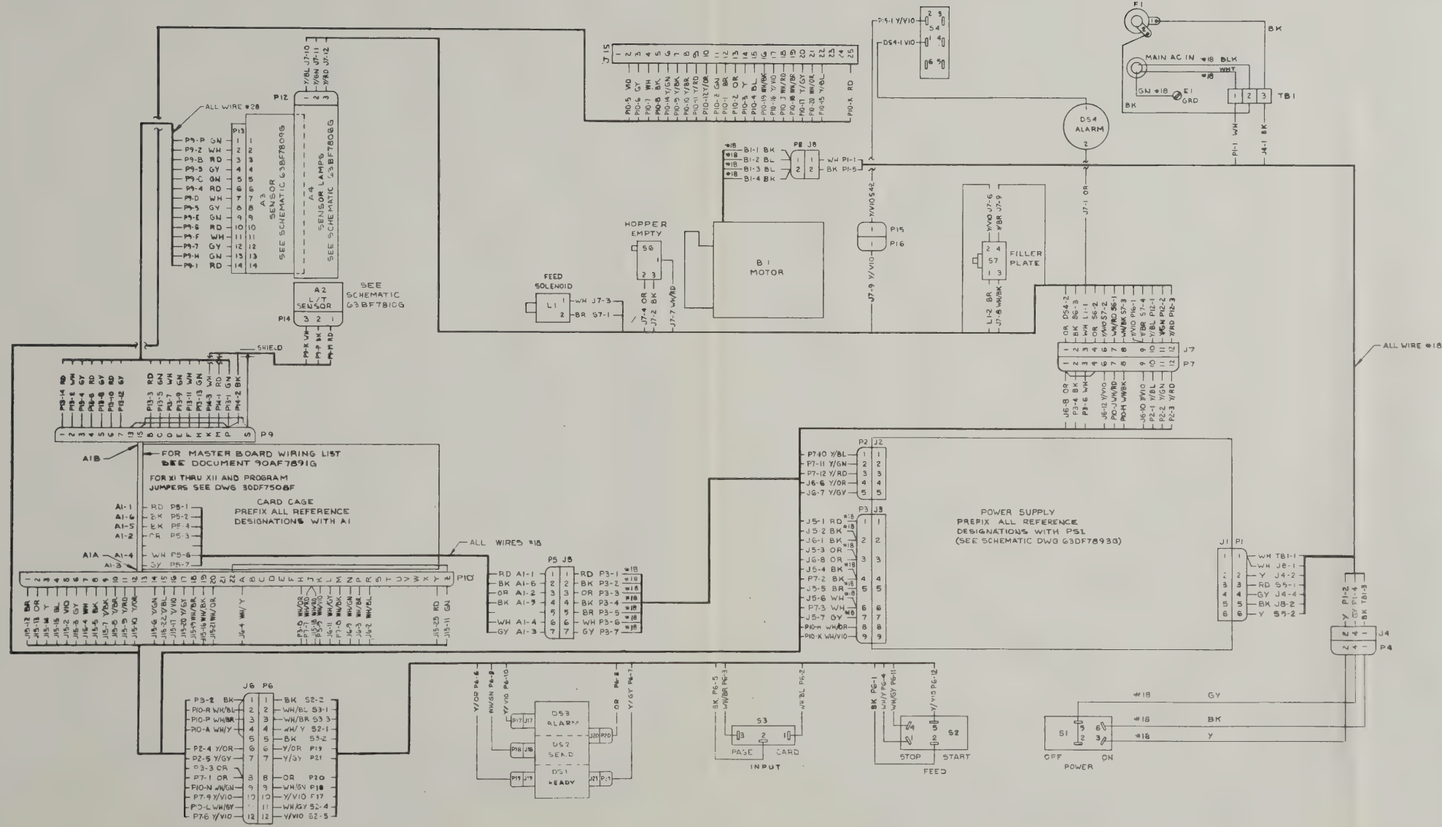


FIGURE 50
MDR PARALLEL WIRING DIAGRAM



(DWG. NO. 90DF7551H)

FIGURE 50
MDR PARALLEL WIRING DIAGRAM

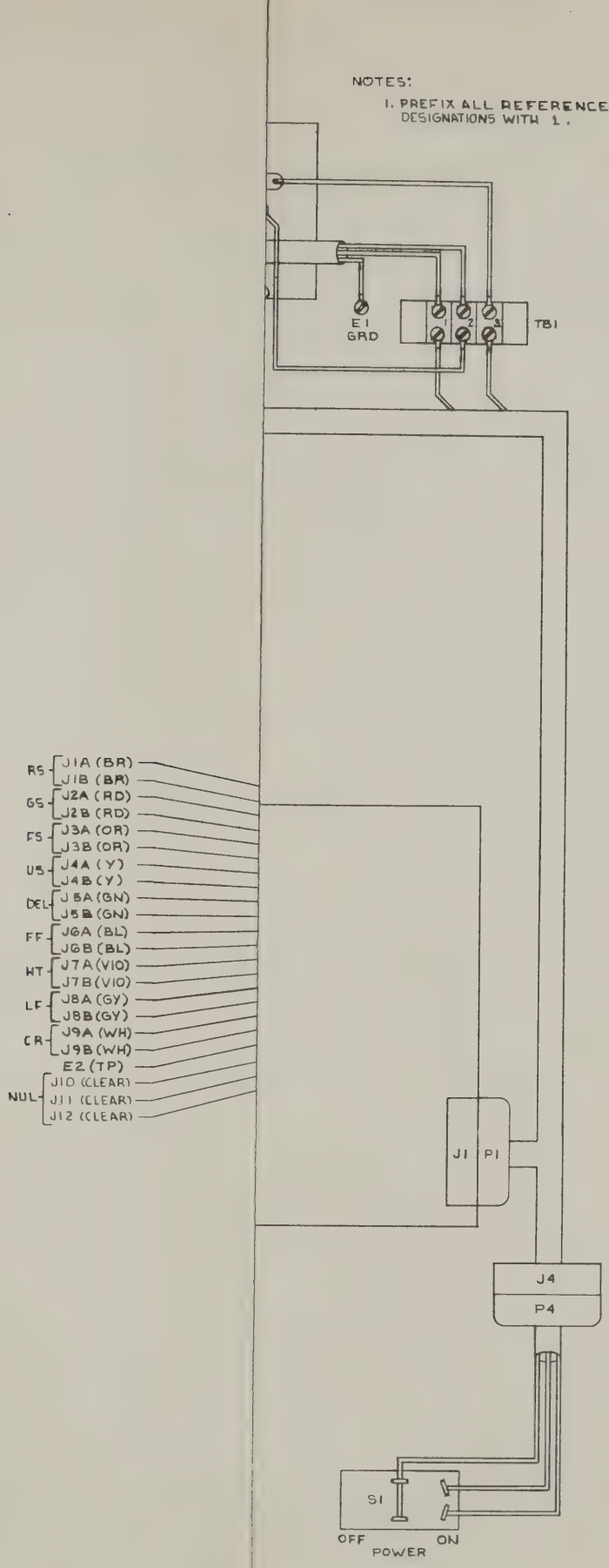
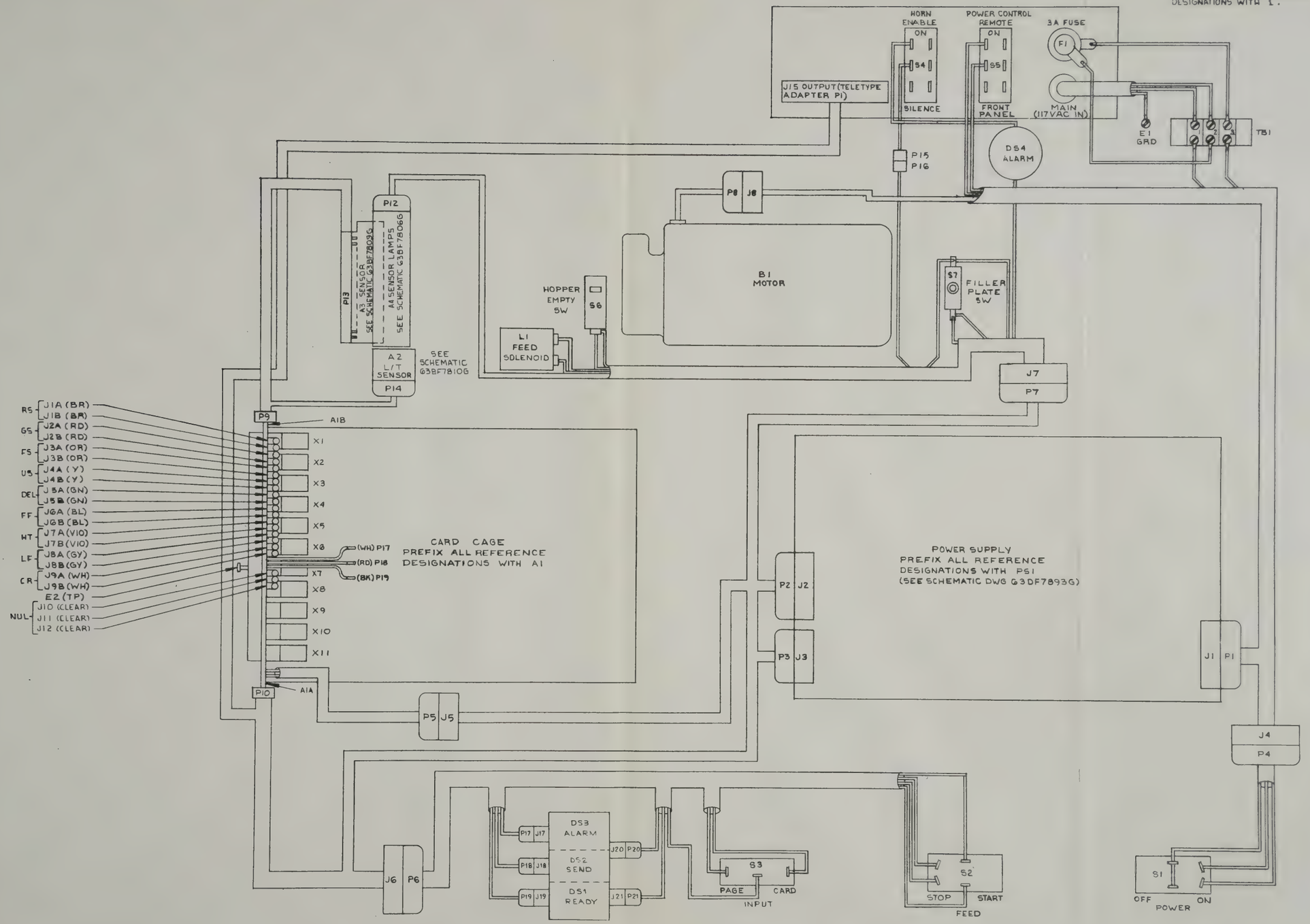


FIGURE 51
MDR SERIAL CABLING DIAGRAM

NOTES:
1. PREFIX ALL REFERENCE DESIGNATIONS WITH 1.



(DWG. NO. 30DF7508F)

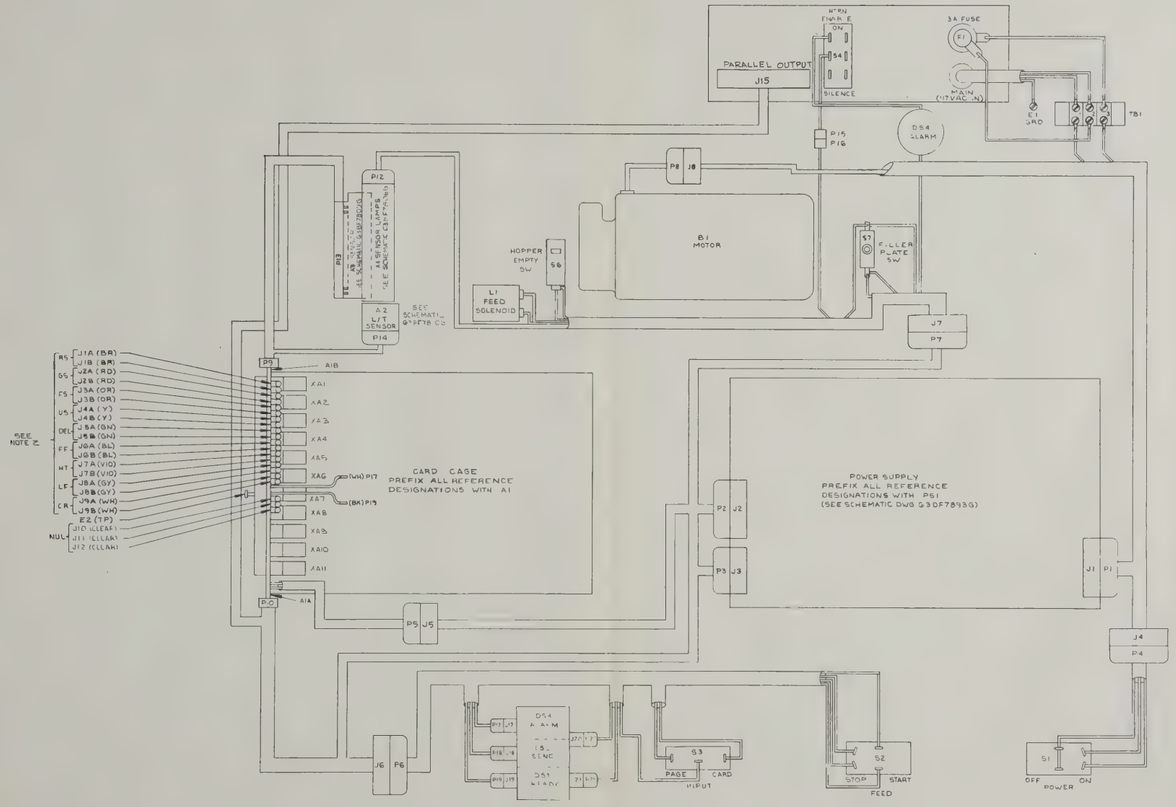
FIGURE 51
MDR SERIAL CABLING DIAGRAM

NOTES:

1. PREFIX ALL REFERENCE DESIGNATIONS WITH 1.
2. ONLY APPLIES TO HOLLERITH USASC DECODER.

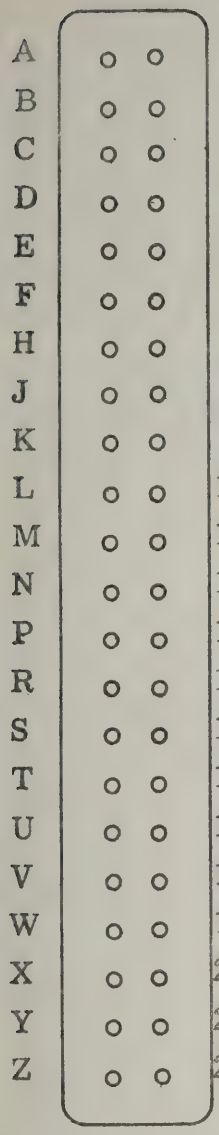
FIGURE 52
MDR PARALLEL CABLING DIAGRAM

NOTE:
1. PREFIX ALL REFERENCE DESIGNATIONS WITH 'E'.
2. ONLY APPLIES TO HOLLERITH BASE DECODER.

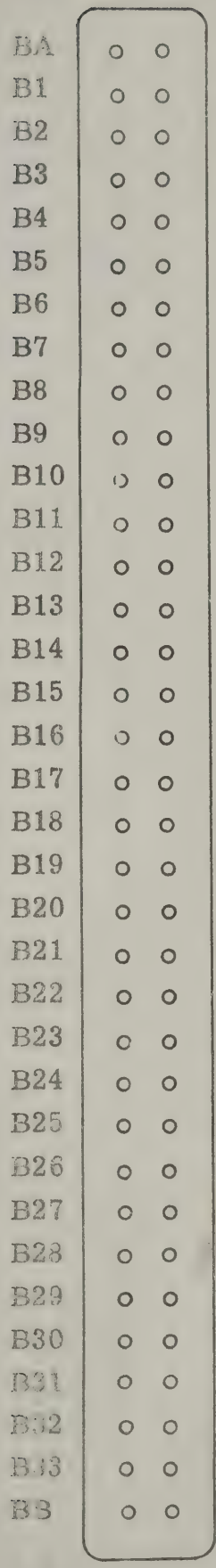


(DWG. NO. 30DF7553H)

FIGURE 52
MDR PARALLEL CABLING DIAGRAM

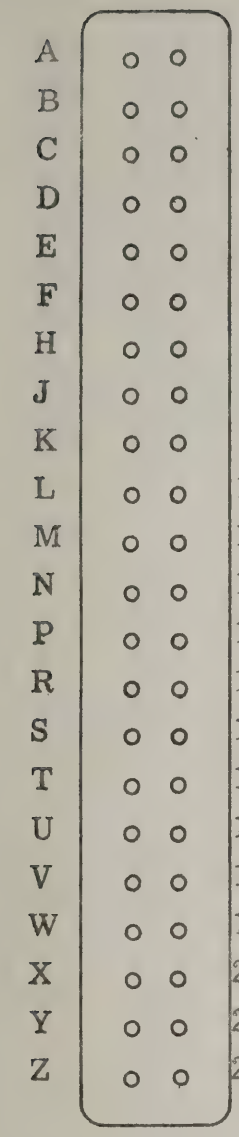


44-Pin Connector
(Rear View)

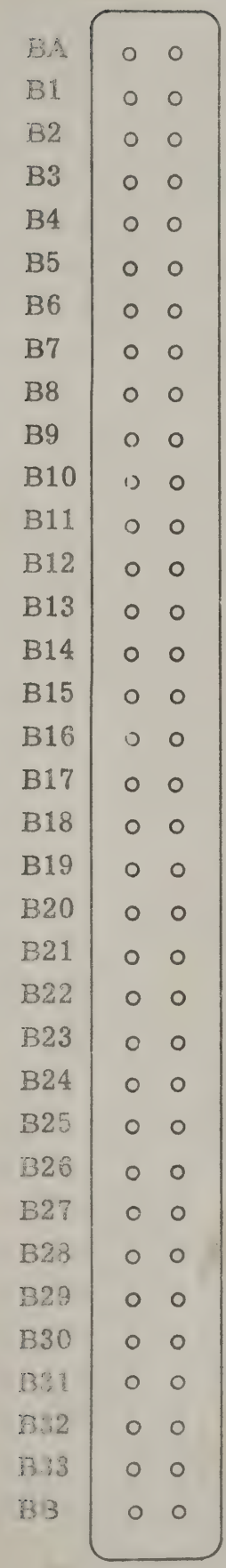


70-Pin Connector
(Rear View)

CONNECTOR PIN NUMBERS
(P/O FIGURES 53 & 54

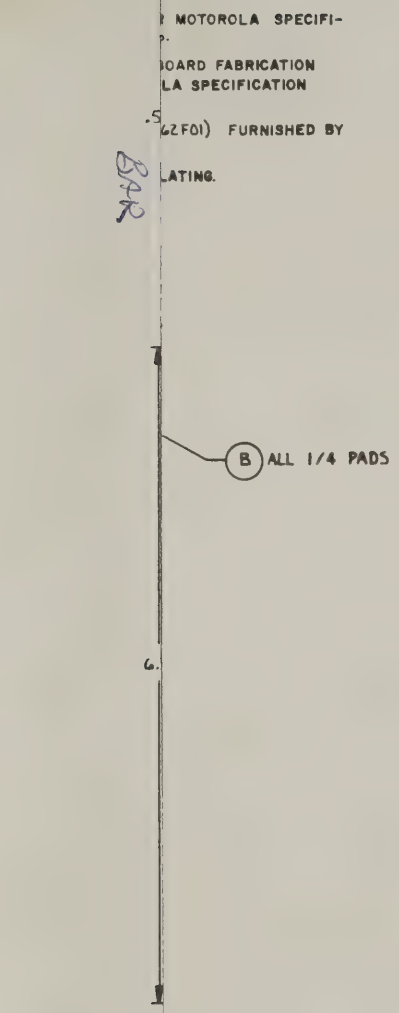


44-Pin Connector
(Rear View)



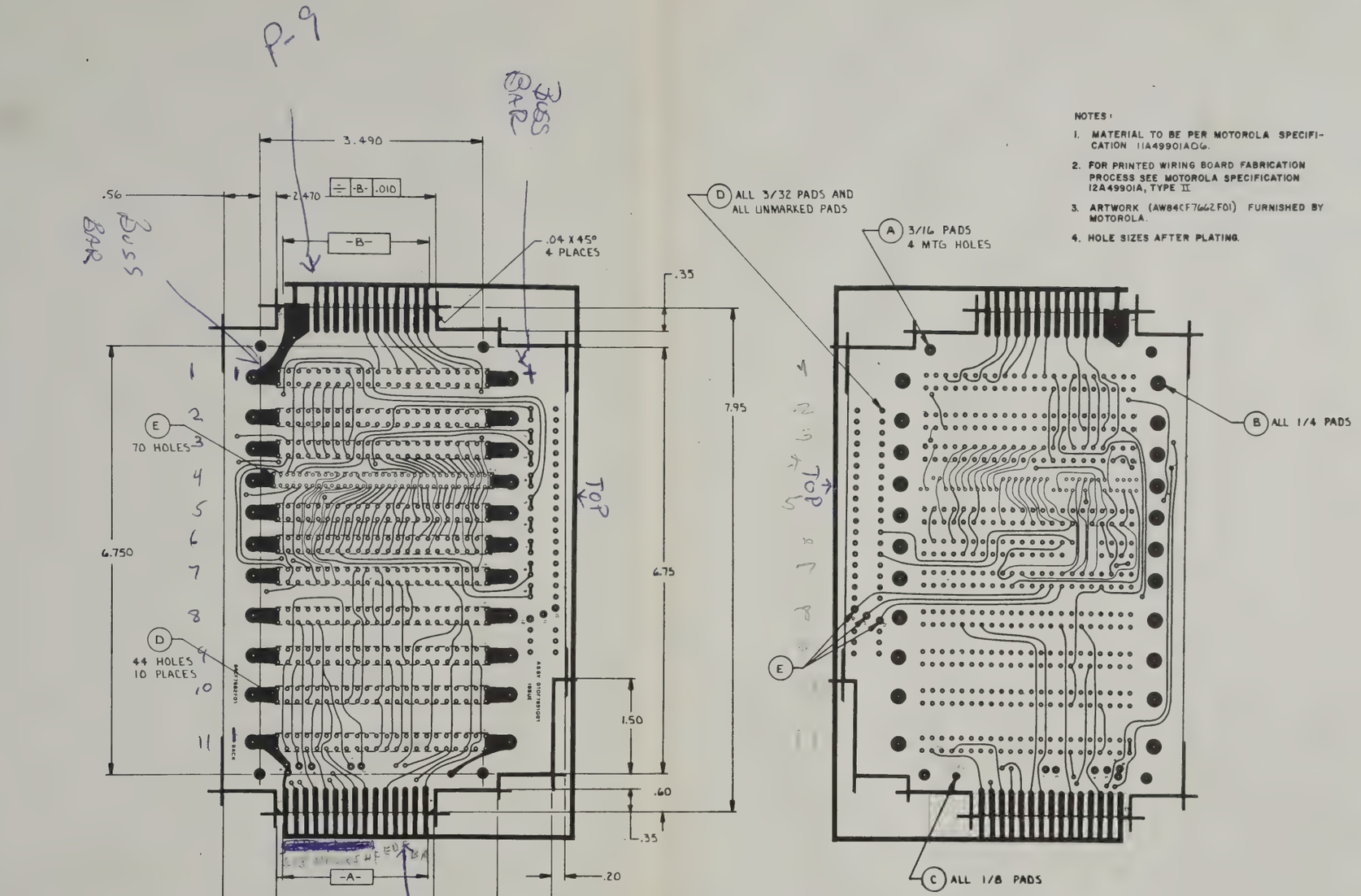
70-Pin Connector
(Rear View)

CONNECTOR PIN NUMBERS
(P/O FIGURES 53 & 54



E	.039 ± .002
D	.050 ± .002
C	.055 ± .002
B	.147 DIA
A	.177 DIA
SYM	DESCR
	HOLE

FIGURE 53
MDR SERIAL MASTERBOARD
PRINTED WIRING LAYOUT



SYM	DESCRIPTION	QTY
HOLE LIST		
A	.177 DIA	4
B	.147 DIA	22
C	.055 ± .002 DIA	7
D	.050 ± .002 DIA	500
E	.039 ± .002 DIA	73

(DWG NO. 84CF7662F)

FIGURE 53
MDR SERIAL MASTERBOARD
PRINTED WIRING LAYOUT

TERIAL TO BE PER MOTOROLA SPECIFI-
TION 11A49901A06.

PRINTED WIRING BOARD FABRICATION
OCESS SEE MOTOROLA SPECIFICATION
49901A, TYPE II

TWORK (AW84CF72B3H01) FURNISHED BY
TOROLA.

LE SIZES AFTER PLATING.

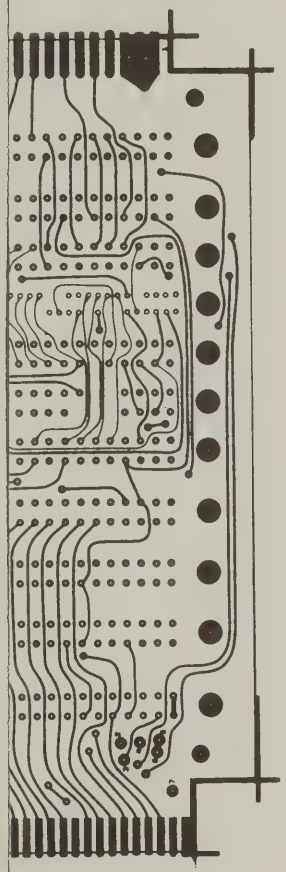
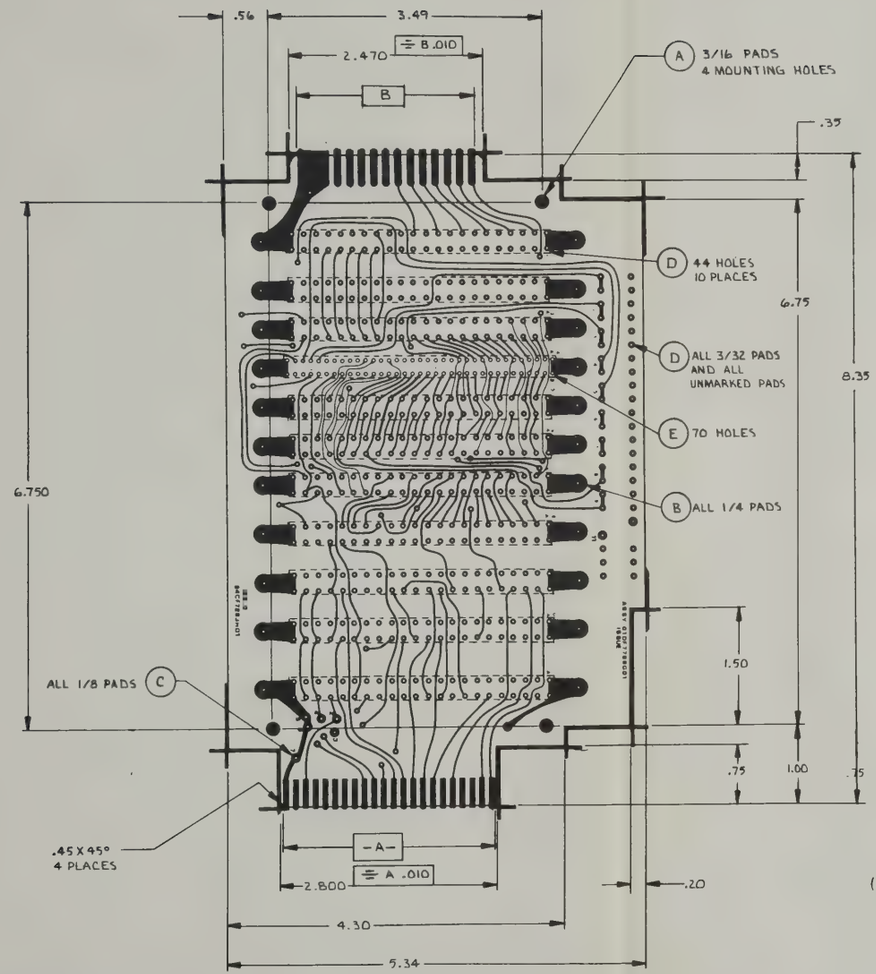


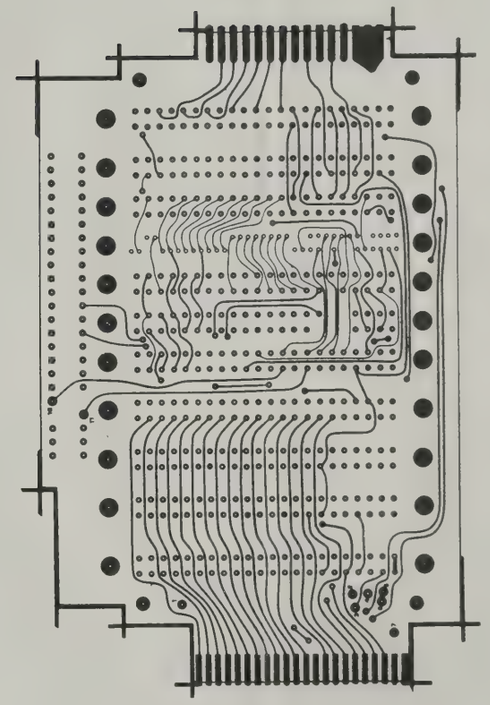
FIGURE 54
MDR PARALLEL MASTERBOARD
PRINTED WIRING LAYOUT

NOTES:

1. MATERIAL TO BE PER MOTOROLA SPECIFICATION 11A49901A06.
2. FOR PRINTED WIRING BOARD FABRICATION PROCESS SEE MOTOROLA SPECIFICATION 12A49901A, TYPE II
3. ARTWORK (AW84CF7283H01) FURNISHED BY MOTOROLA
4. HOLE SIZES AFTER PLATING.



E	.039 ± .002 DIA	70
D	.050 ± .002 DIA	500
C	.072 ± .002 DIA	10
B	.147 DIA	22
A	.177 DIA	4
SYM	[illegible]	QTY



(DWG. NO. 84CF7283H)

FIGURE 54
MDR PARALLEL MASTERBOARD
PRINTED WIRING LAYOUT

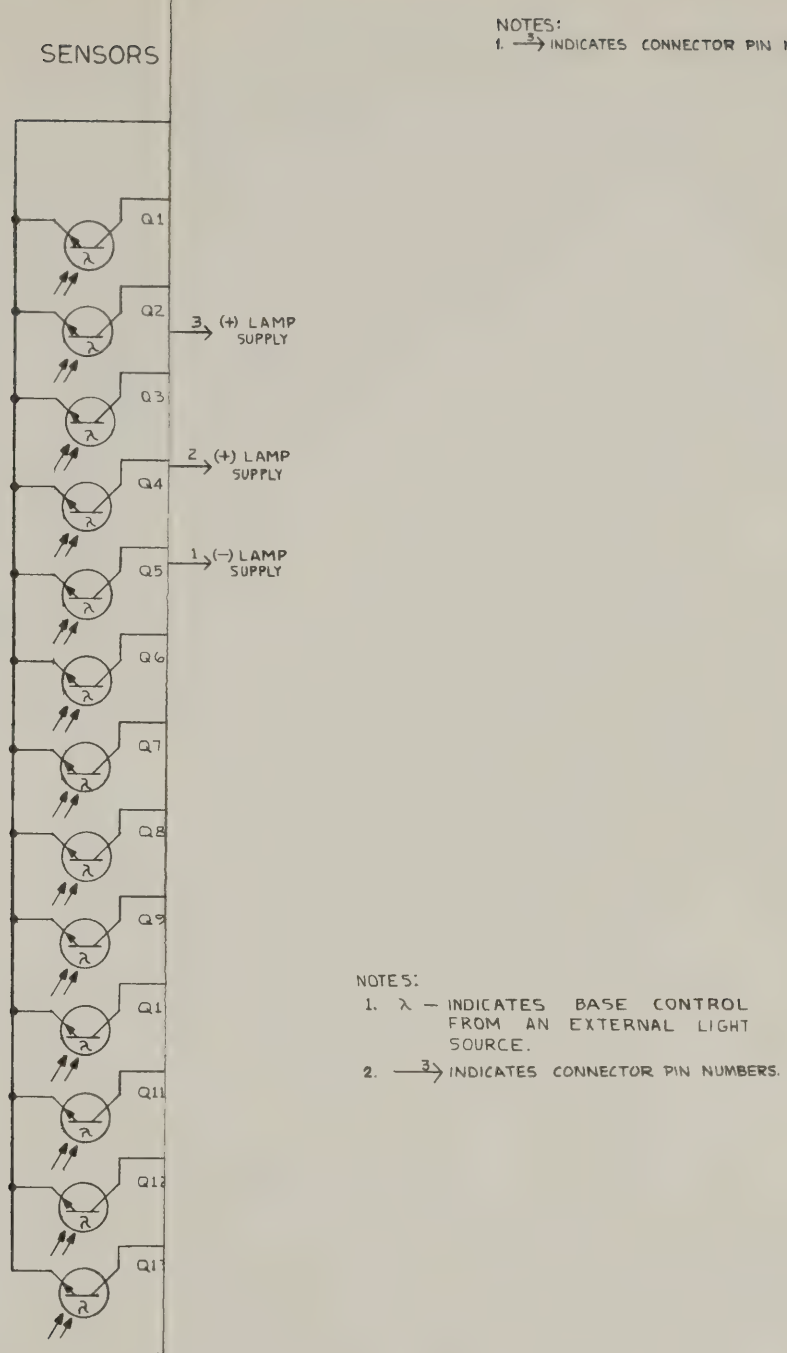
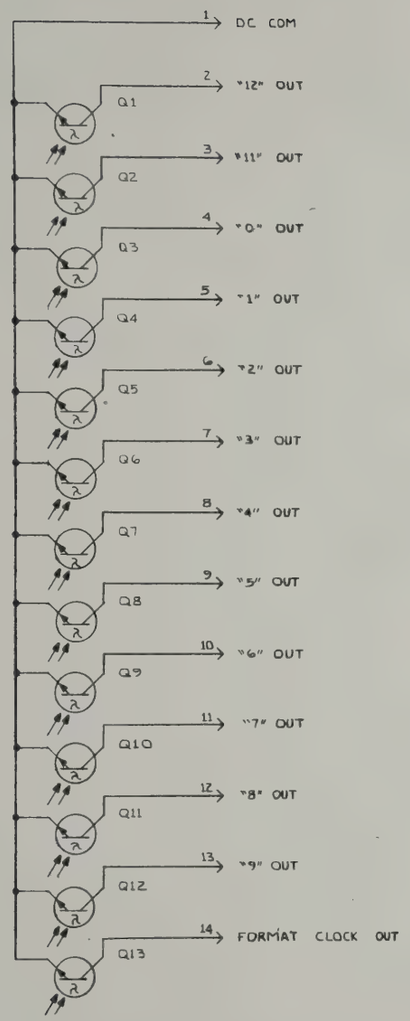


FIGURE 55
SENSOR HEAD SCHEMATIC DIAGRAM

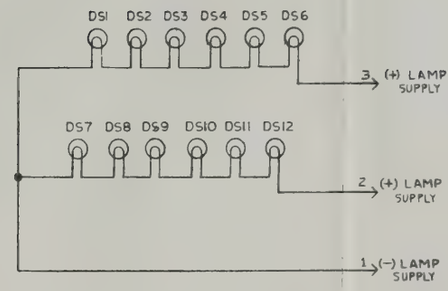
SENSORS



(DWG. NO. 63BF7809G)

NOTES:
1. λ — INDICATES BASE CONTROL FROM EXTERNAL LIGHT SOURCE.
2. —3→ INDICATES CONNECTOR PIN NUMBERS.

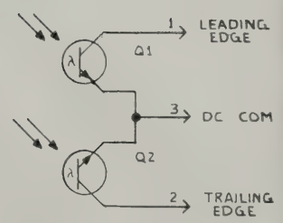
SENSOR LAMP



(DWG. NO. 63BF/806G)

NOTES:
1. —3→ INDICATES CONNECTOR PIN NUMBERS.

L/T SENSOR



(DWG. NO. 63BF7810G)

NOTES:
1. λ — INDICATES BASE CONTROL FROM AN EXTERNAL LIGHT SOURCE.
2. —3→ INDICATES CONNECTOR PIN NUMBERS

FIGURE 55
SENSOR HEAD SCHEMATIC DIAGRAM

AR1 THRU AR12 DETAIL

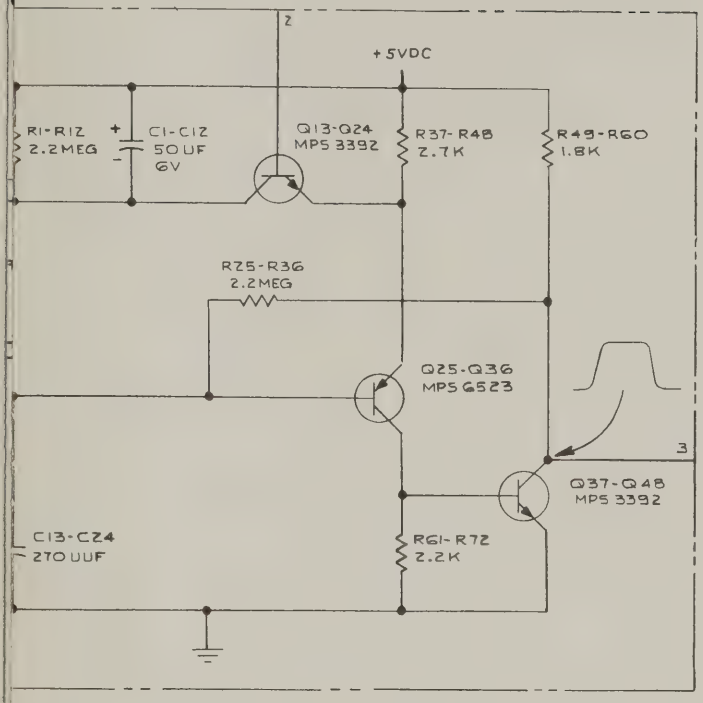
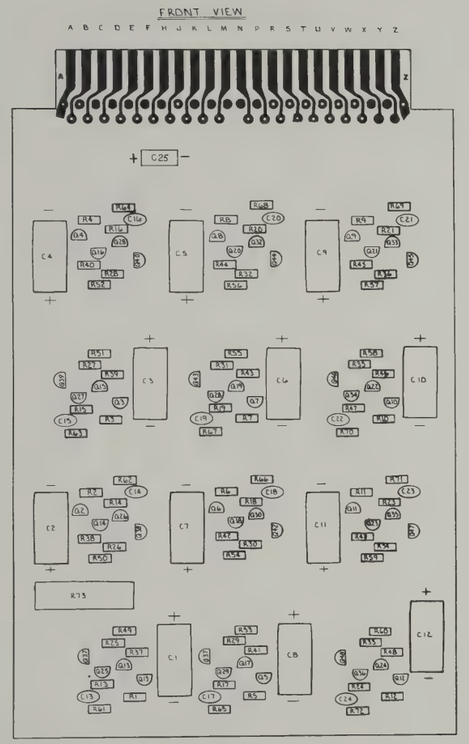
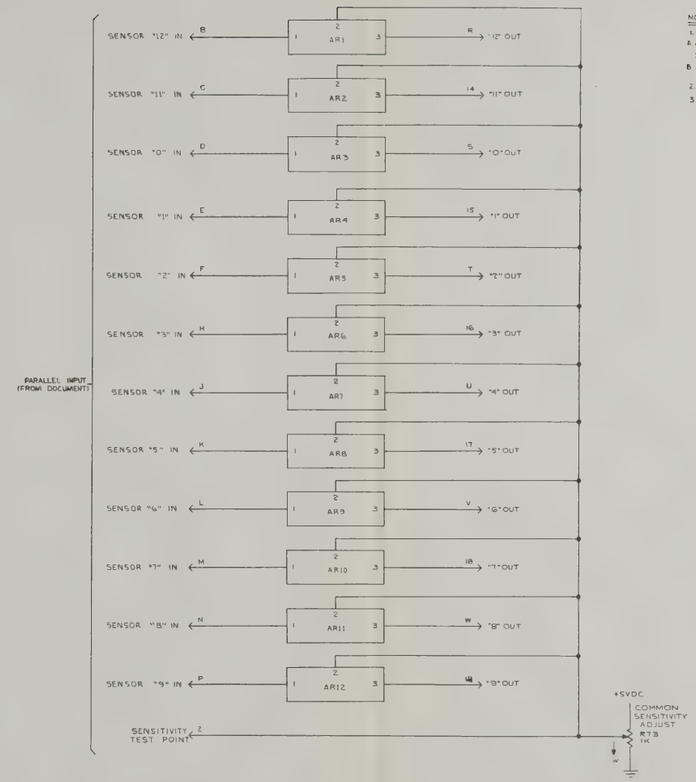


FIGURE 56
DATA ROW SENSOR AMPLIFIERS
SCHEMATIC DIAGRAM & COMPONENT LOCATION



(DWG. NO. 01CF1870G)



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS ± 10 PCT, 1/4 WATT.
   B. ALL WAVE FORMS ARE 5VP-P (0VDC TO +5VDC)
2. POSITIVE LOGIC USED
3. (XX), (ZZ) INDICATE CONNECTOR PIN NUMBERS

(DWG. NO. 63DF7870G)

AR1 THRU AR12 DETAIL

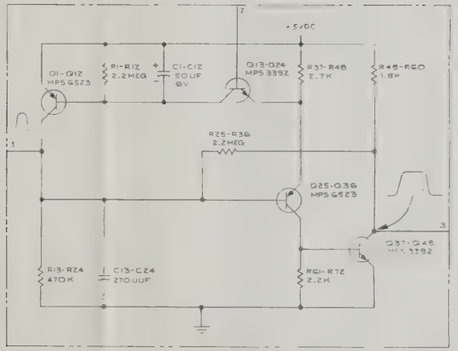


FIGURE 56
DATA ROW SENSOR AMPLIFIERS
SCHEMATIC DIAGRAM & COMPONENT LOCATION

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS ± 10PCT, 1/2 WATT.
   B. ALL CAPACITORS ARE IN MICROFARADS.
   C. ALL DIODES ARE SD107.
   D. ALL WAVE FORMS ARE 5VP-P (0VDC TO +5VDC)
2. POSITIVE LOGIC USED.
3. $\xrightarrow{22}$, $\xrightarrow{7}$ INDICATE CONNECTOR PIN NUMBERS.

ILING EDGE (T.E.) AMPLIFIER

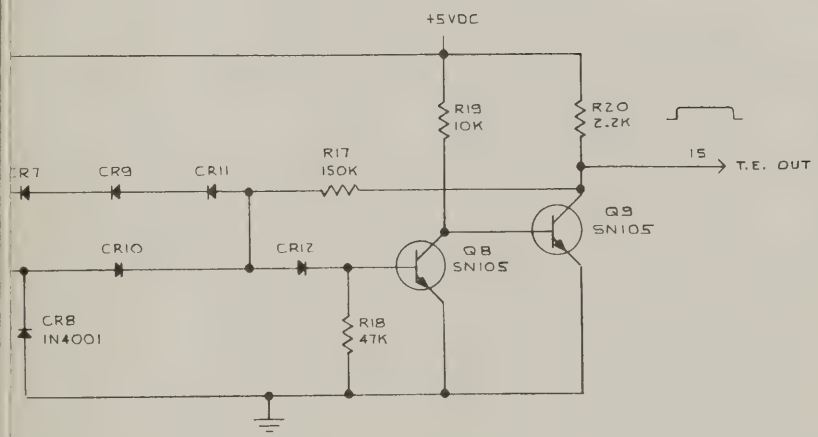
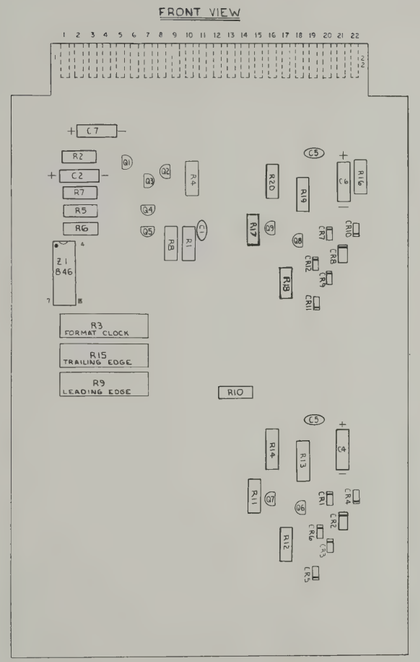


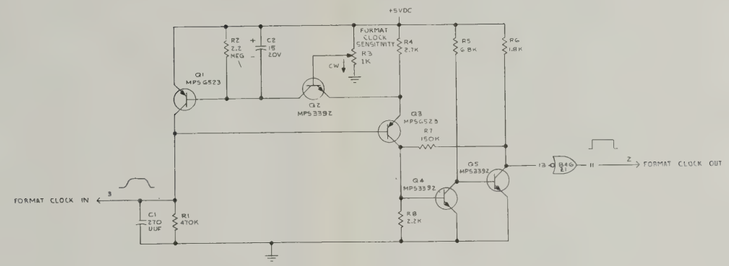
FIGURE 57
L/T & CLOCK AMPLIFIERS
SCHEMATIC DIAGRAM & COMPONENT LOCATION



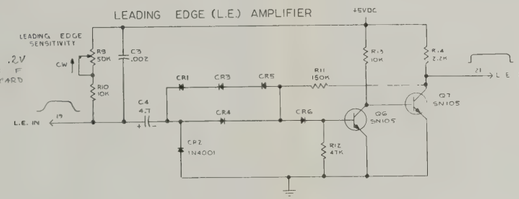
(DWG. NO. 01CF7871G)

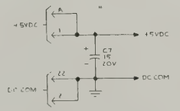
FORMAT CLOCK AMPLIFIER

.2V P-P (MIN) CARD



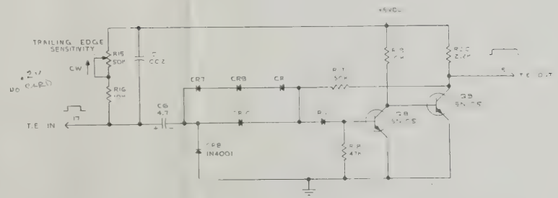
LEADING EDGE (L.E.) AMPLIFIER





(DWG. NO. 63DF7871G)

TRAILING EDGE (T.E.) AMPLIFIER



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE IN OHMS, ± 10PCT, 1/4 WATT
2. ALL CAPACITORS ARE IN MICROFARADS
3. ALL DIODES ARE 1N4001
4. ALL WAVE FORMS ARE 5VP-P (0VDC TO +5VDC)
5. POSITIVE LOGIC USED
6. (XX), XX INDICATE CONNECTOR PIN NUMBERS

FIGURE 57
L/T & CLOCK AMPLIFIERS
SCHEMATIC DIAGRAM & COMPONENT LOCATION

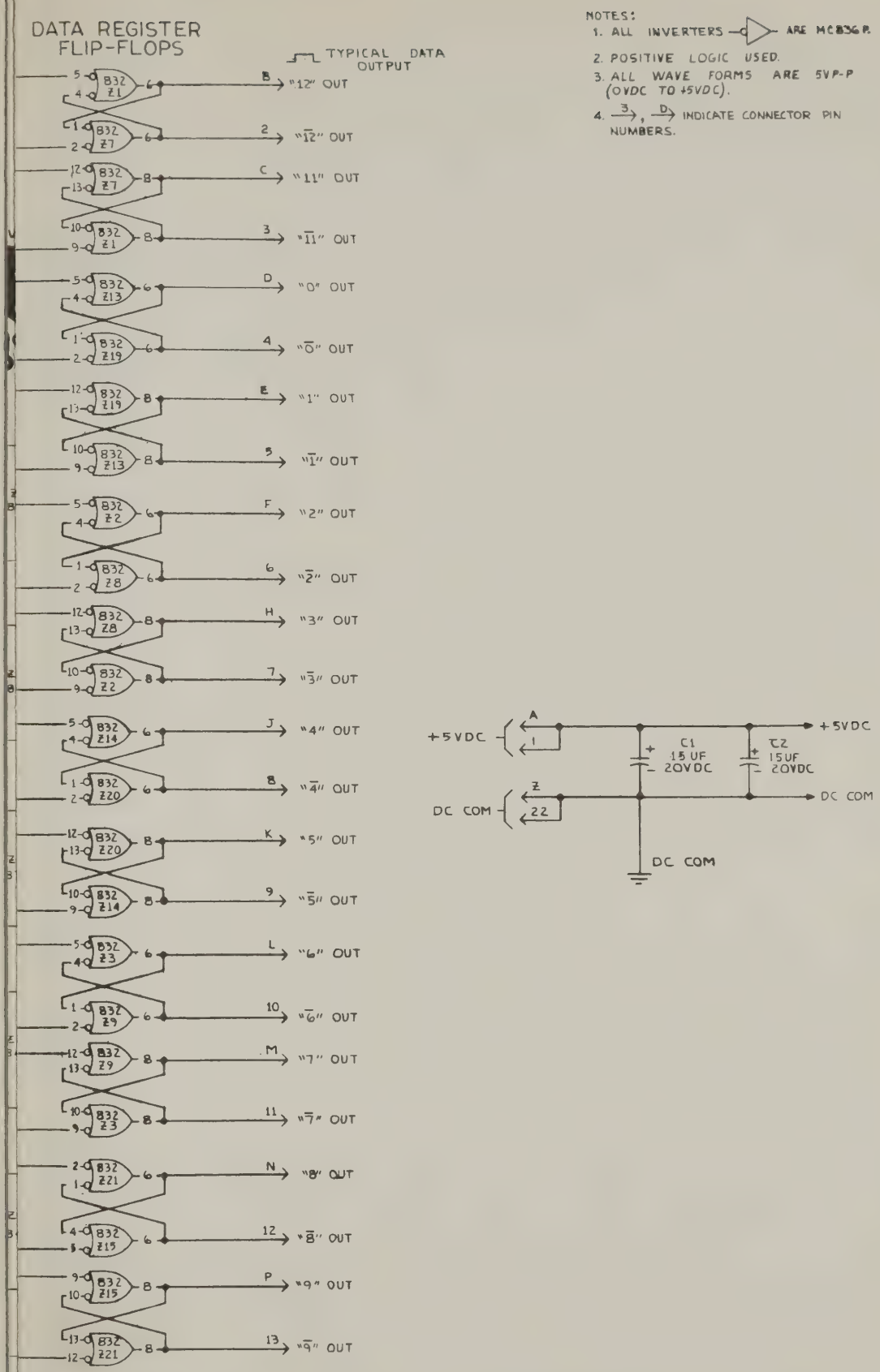
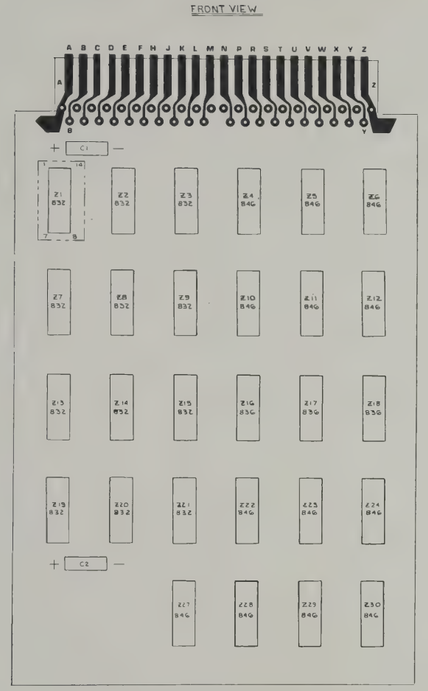
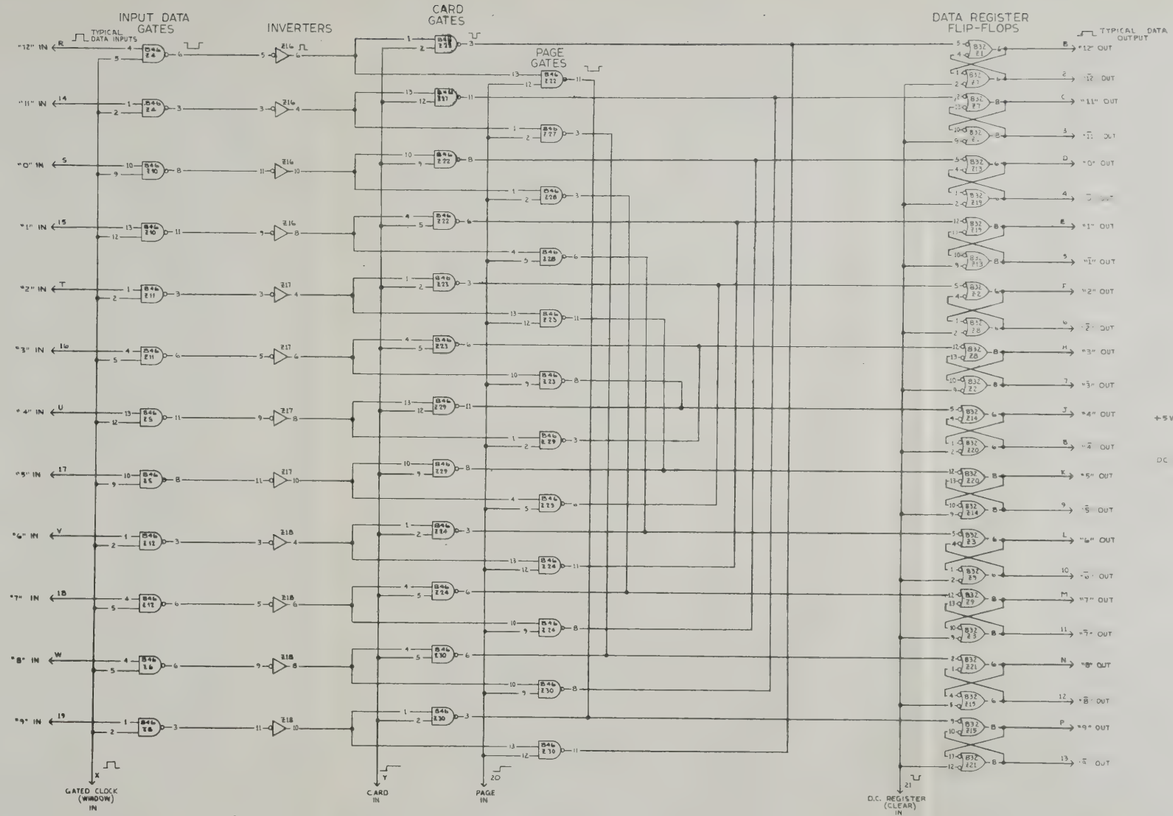


FIGURE 58
DATA REGISTERS W/INVERSION
SCHEMATIC DIAGRAM & COMPONENT LOCATION



(DWG. NO. 01CF7873G)



(DWG. NO. 63DF7873G)

NOTES:
1. ALL INVERTERS ARE MC85GR
2. POSITIVE LOGIC USED
3. ALL WAVE FORMS ARE 5VP-P (0VDC TO +5VDC)
4. INDICATE CONNECTOR PIN NUMBERS

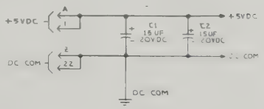


FIGURE 58
DATA REGISTERS W/INVERSION
SCHEMATIC DIAGRAM & COMPONENT LOCATION

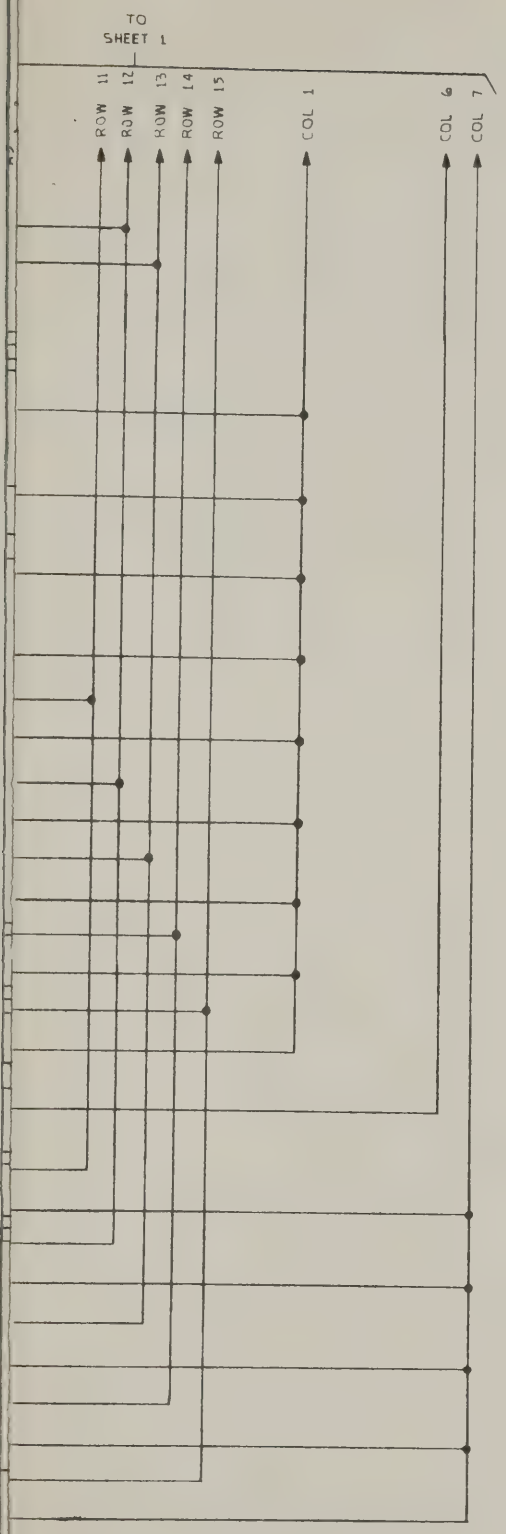
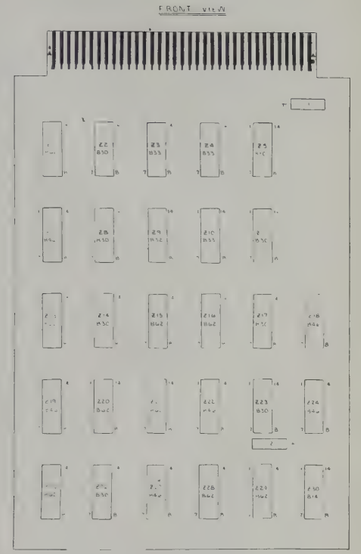
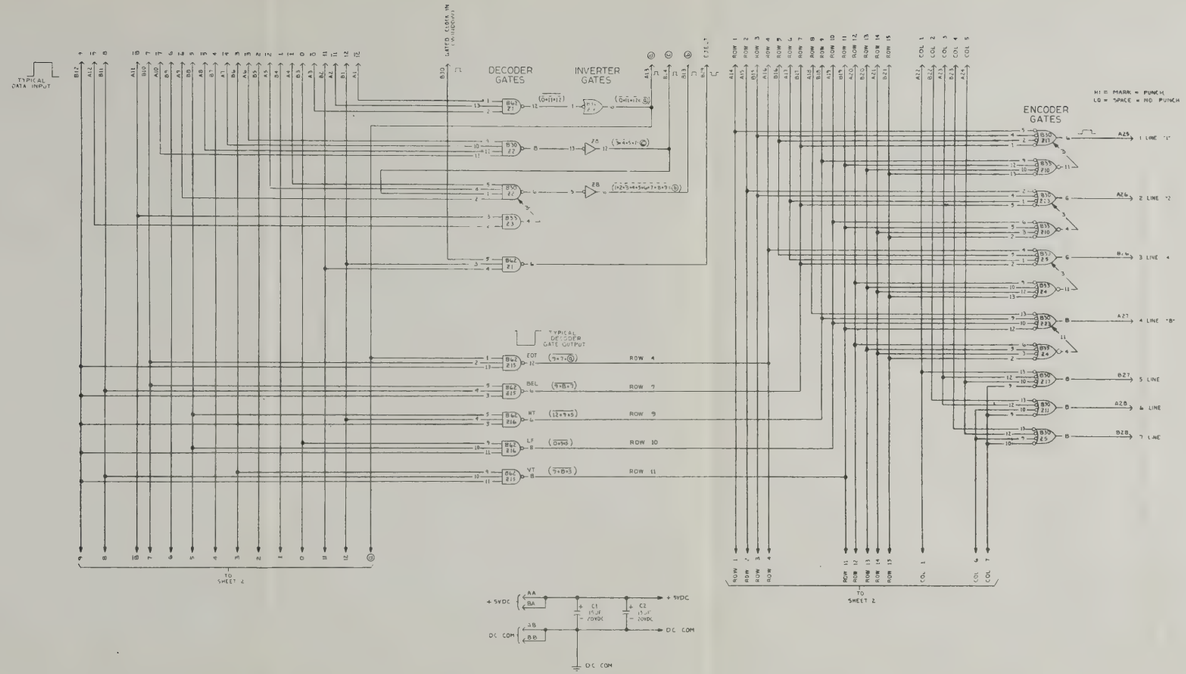


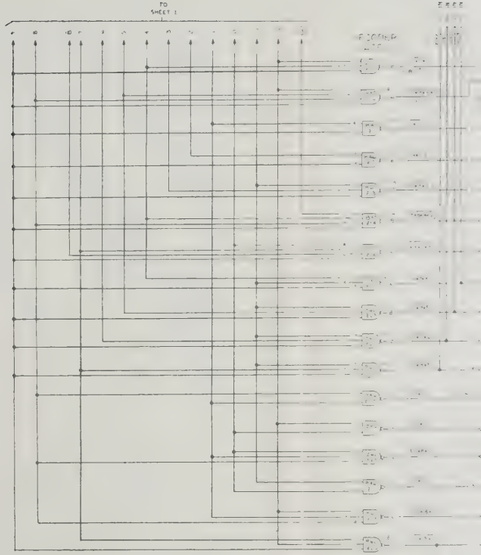
FIGURE 59
HOLL-USASCII, 85 CHAR #1
SCHEMATIC DIAGRAM & COMPONENT LOCATION

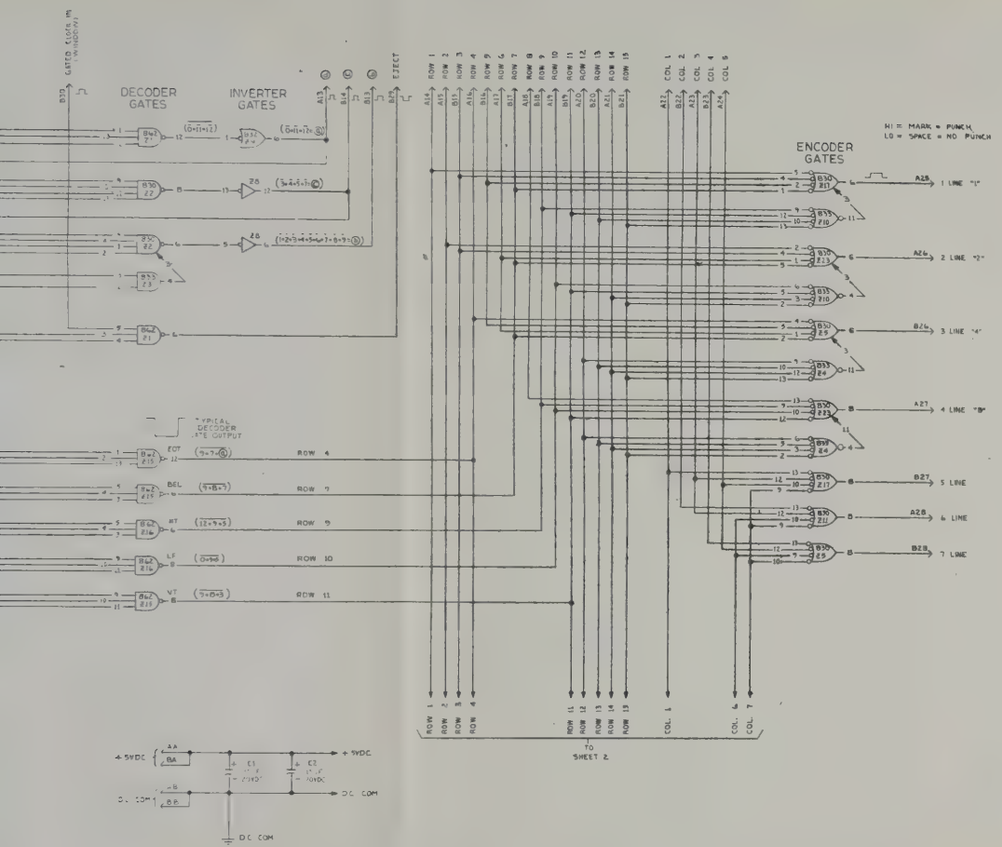


(DWG. NO. 01CF7874G)

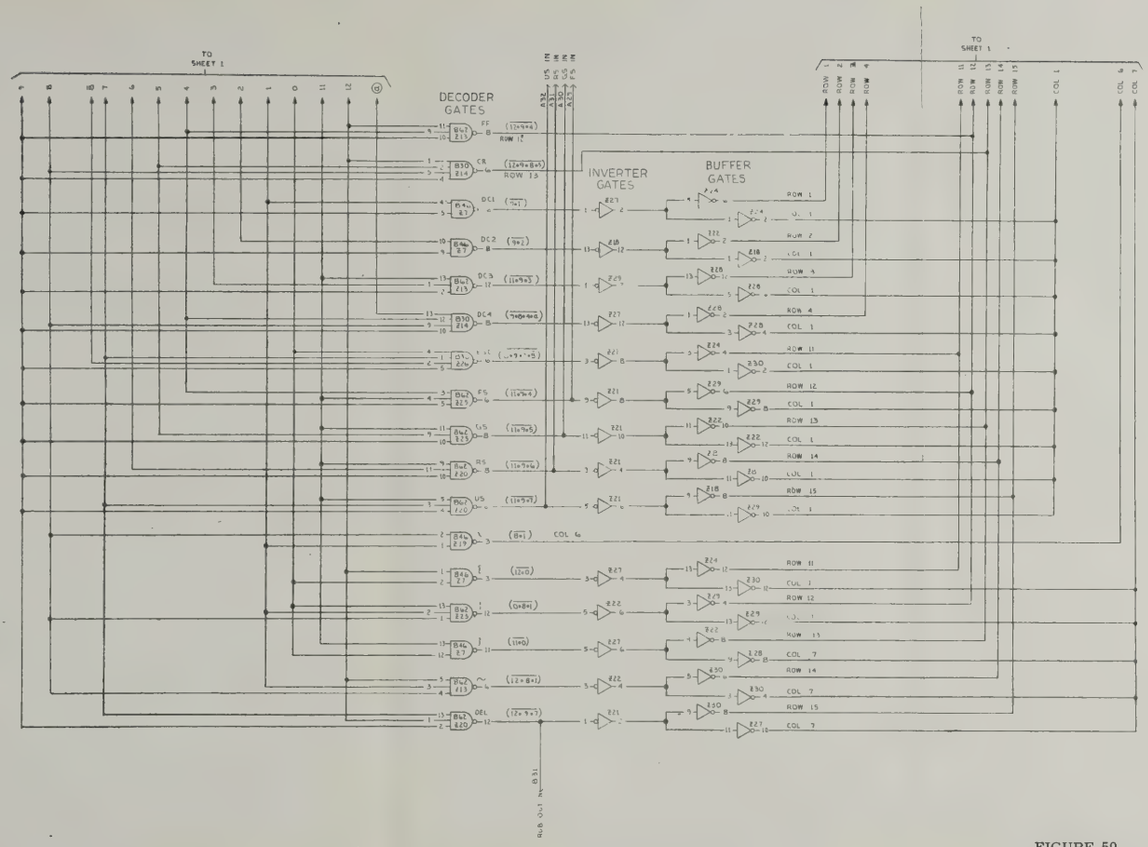


(PIO DWG. NO. 63DF7874G)





(P/O DWG. NO. 63DF7874G)



(P/O DWG. NO. 63DF7874G)

FIGURE 59
HOLL-USASCII, 85 CHAR #1
SCHEMATIC DIAGRAM & COMPONENT LOCATION

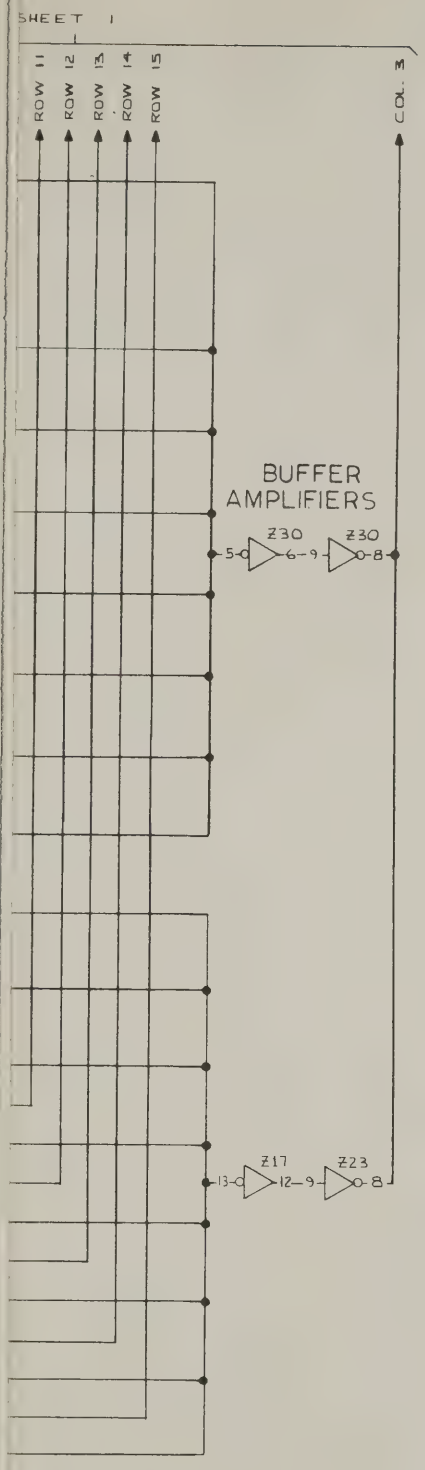
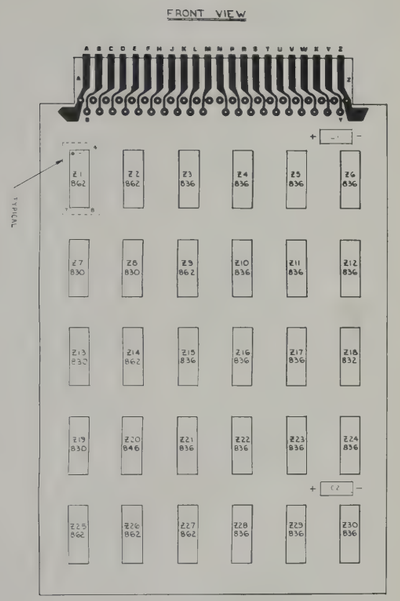
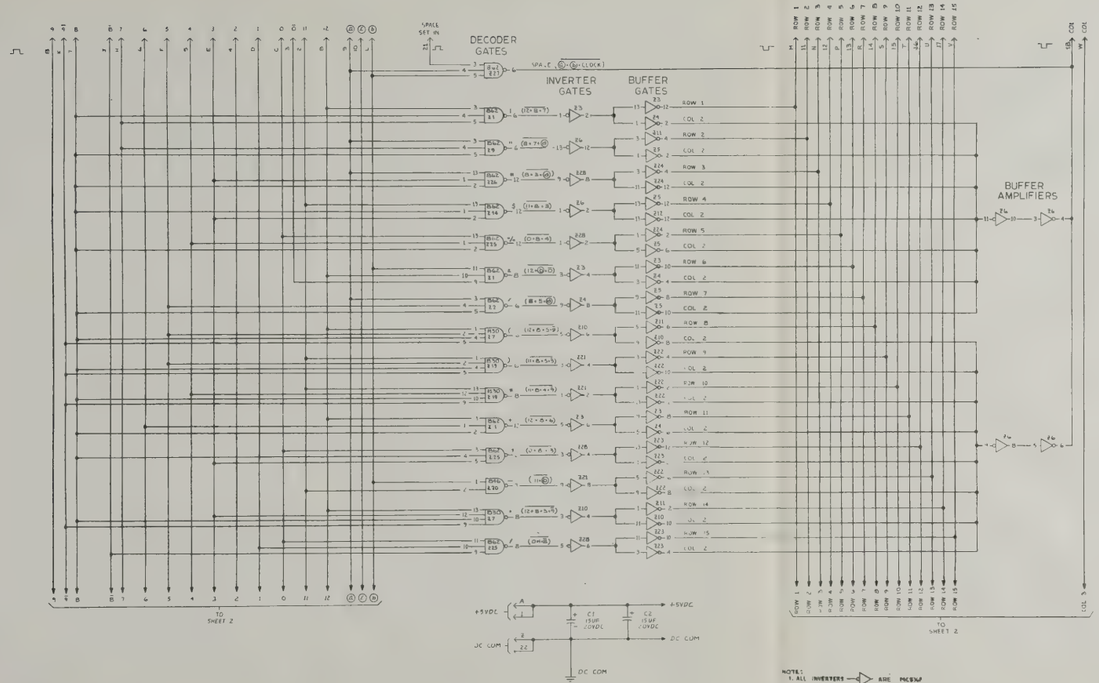


FIGURE 60
HOLL-USASCII, 85 CHAR #2
SCHEMATIC DIAGRAM & COMPONENT LOCATION

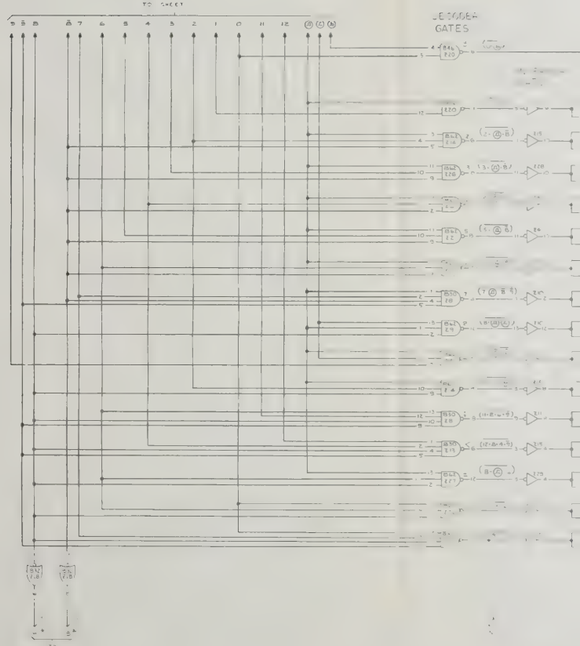


(DWG. NO. 01CF7875C)

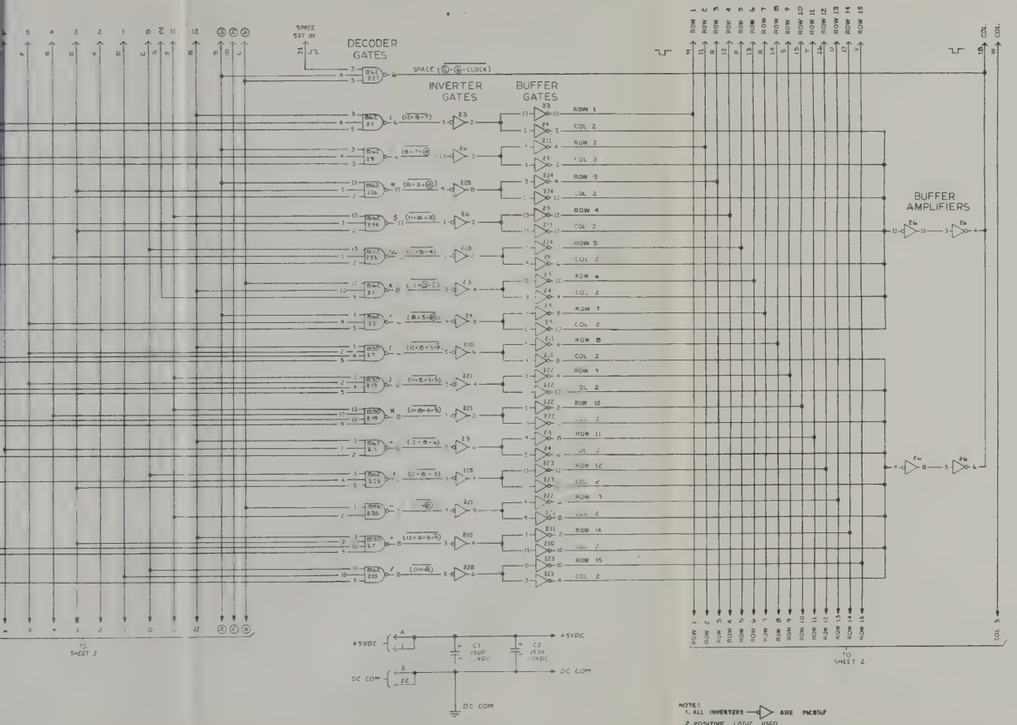


(PIO DWG. NO. 63DF7875C)

NOTES:
1. ALL INVERTERS ARE MC8097
2. POSITIVE LOGIC USED
3. ALL WAVE FORMS ARE SWP-P (0VDC TO 10VDC)
4. (n) INDICATE CONNECTOR PIN NUMBERS



(PIO DWG. NO. 63DF7875C)



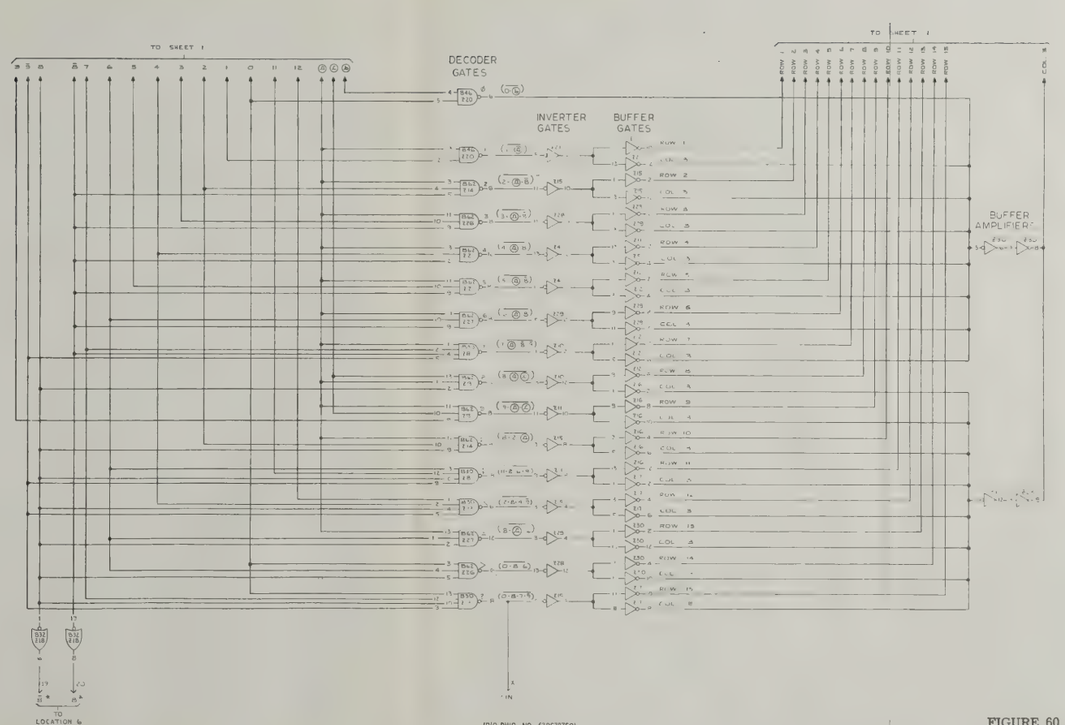


FIGURE 60
HOLL-USASCII, 85 CHAR #2
SCHEMATIC DIAGRAM & COMPONENT LOCATION

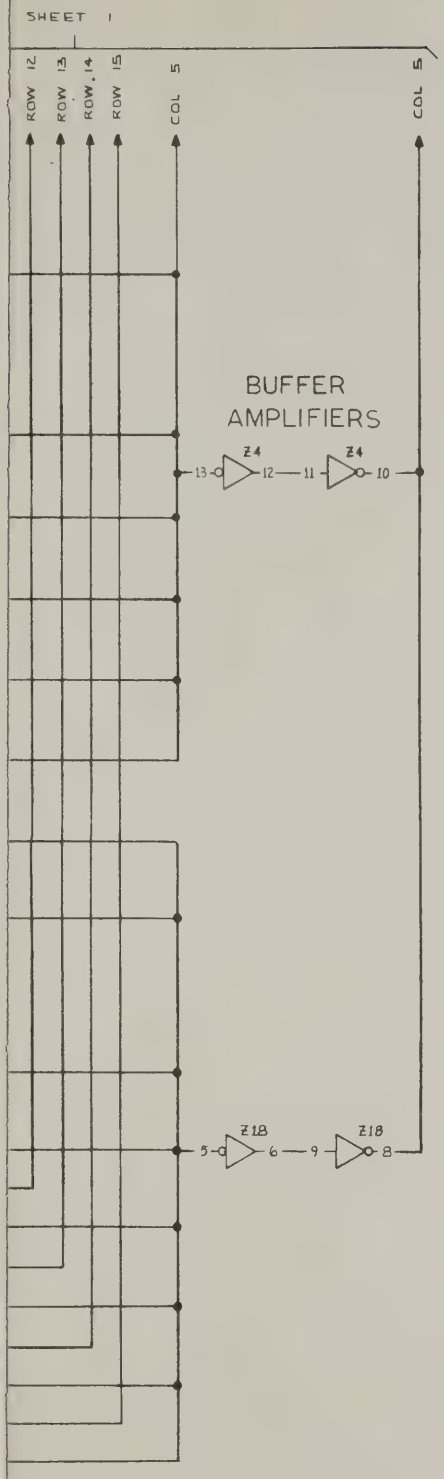
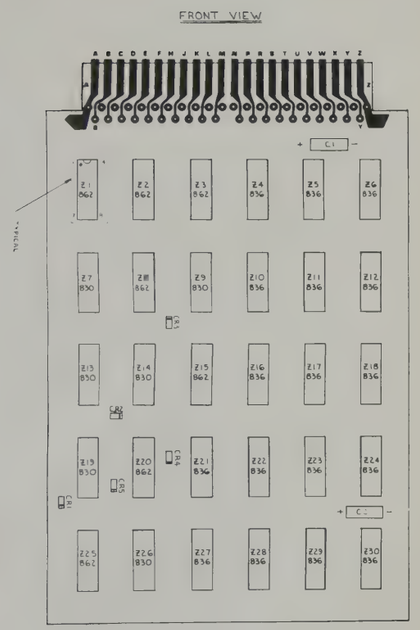
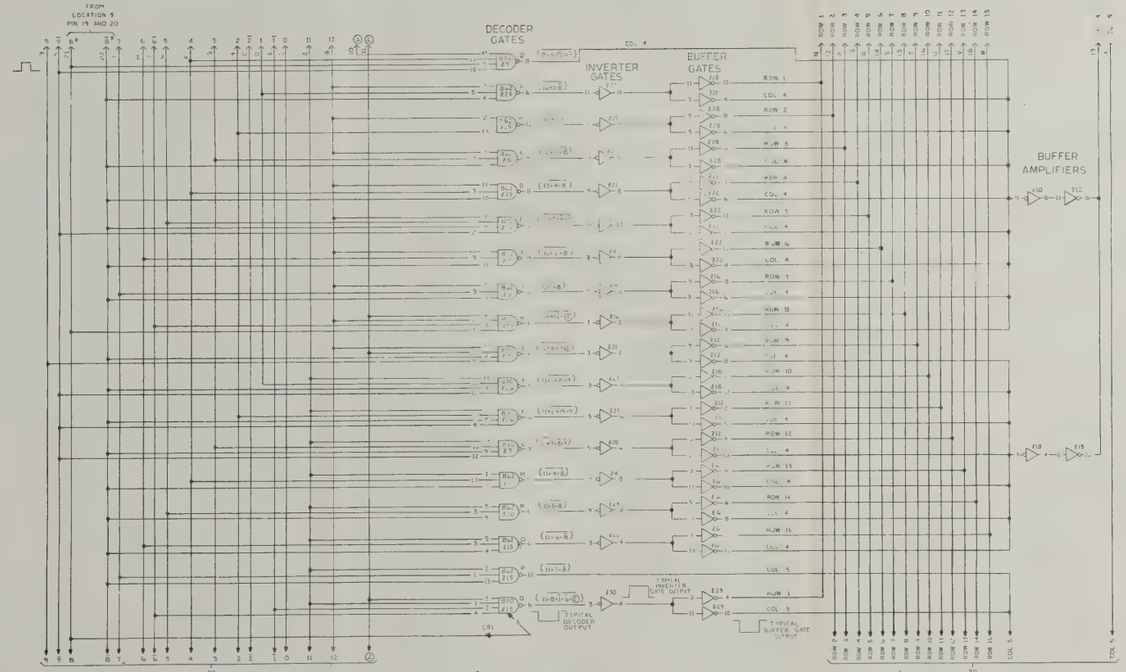
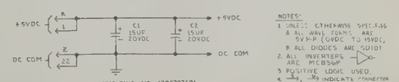


FIGURE 61
HOLL-USASCII, 85 CHAR #3
SCHEMATIC DIAGRAM & COMPONENT LOCATION



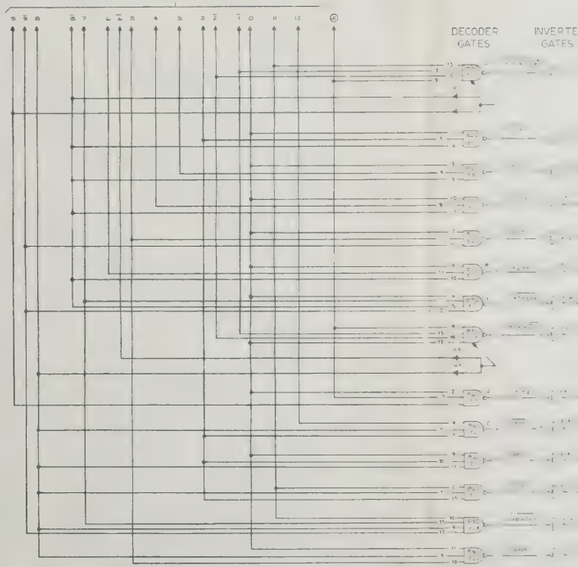
(DWG. NO. 01CF7876G)



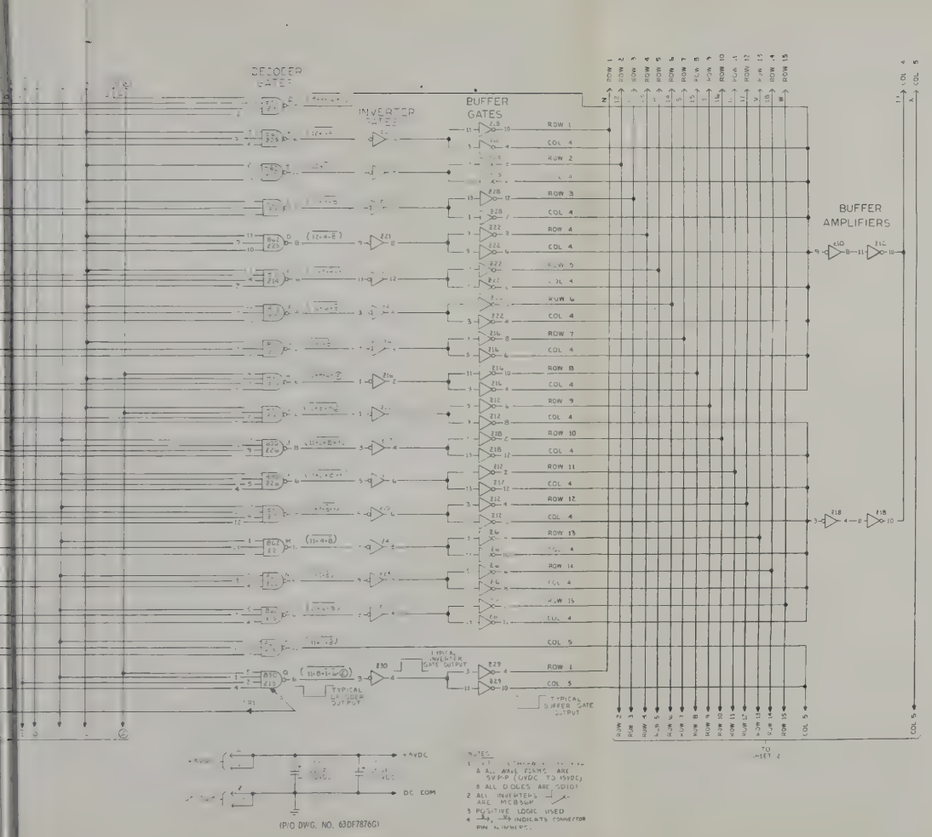


(PIO DWG. NO. 63DF7876G)

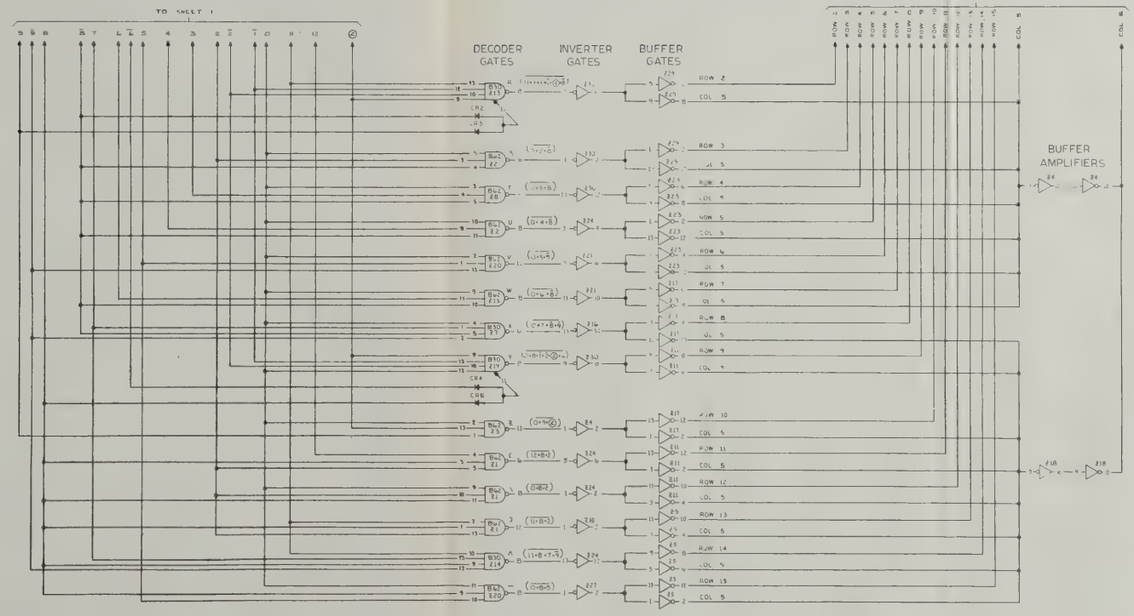
NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL ANALOG SIGNALS ARE 5VP-P (0VDC TO +5VDC, P.P.)
2. ALL DIODES ARE 1N4151
3. ALL INVERTERS ARE MC8304P
4. POSITIVE LOGIC USED.
5. (##) INDICATES CONNECTOR PIN NUMBERS.



(PIO DWG. NO. 63DF7876G)



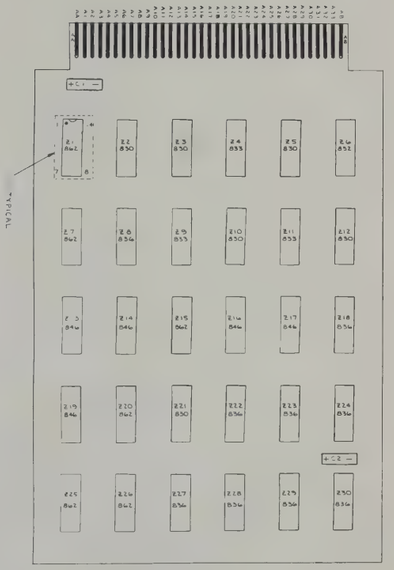
(P/O DWG. NO. 63DF7876G)



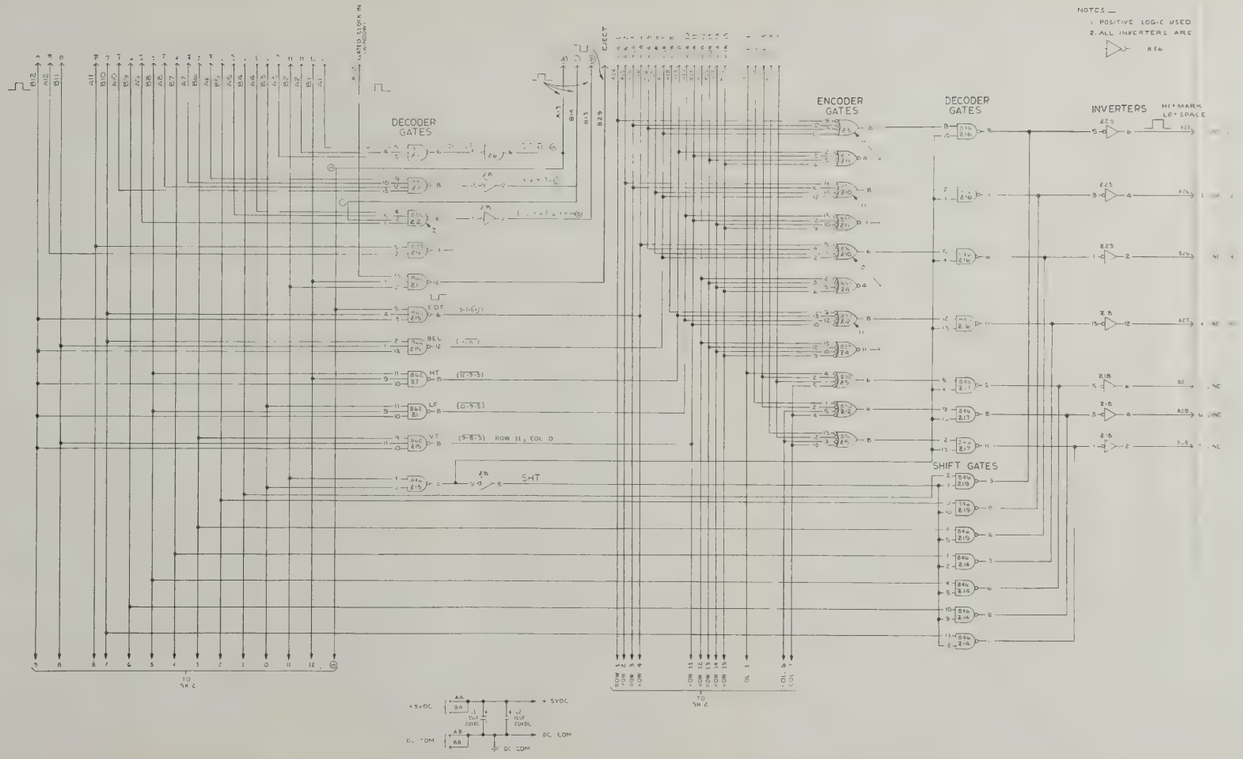
(P/O DWG. NO. 63DF7876G)

FIGURE 61
HOLL-USASCII, 85 CHAR #3
SCHEMATIC DIAGRAM & COMPONENT LOCATION

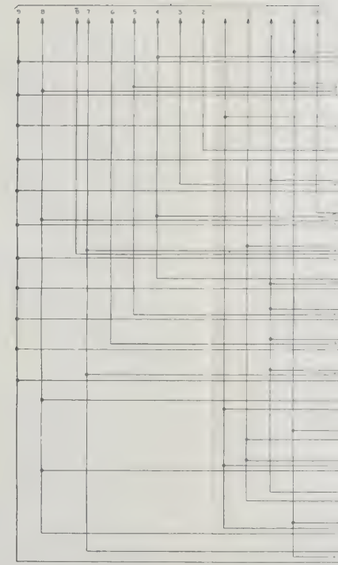
FIGURE 62
HOLL-USASCII, 85 CHAR #1 W/SHIFT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

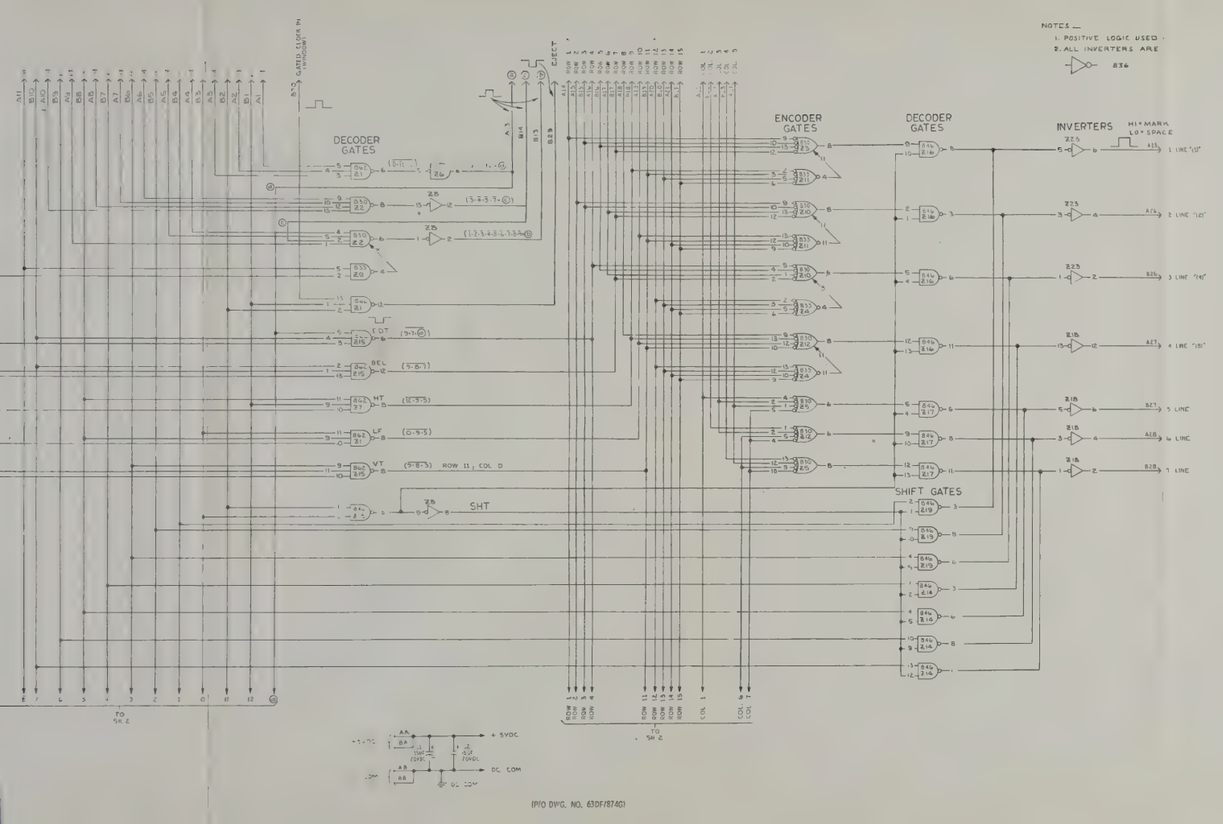


(DWG. NO. 01CF/874G)



(P/O DWG. NO. 63DF/874G)





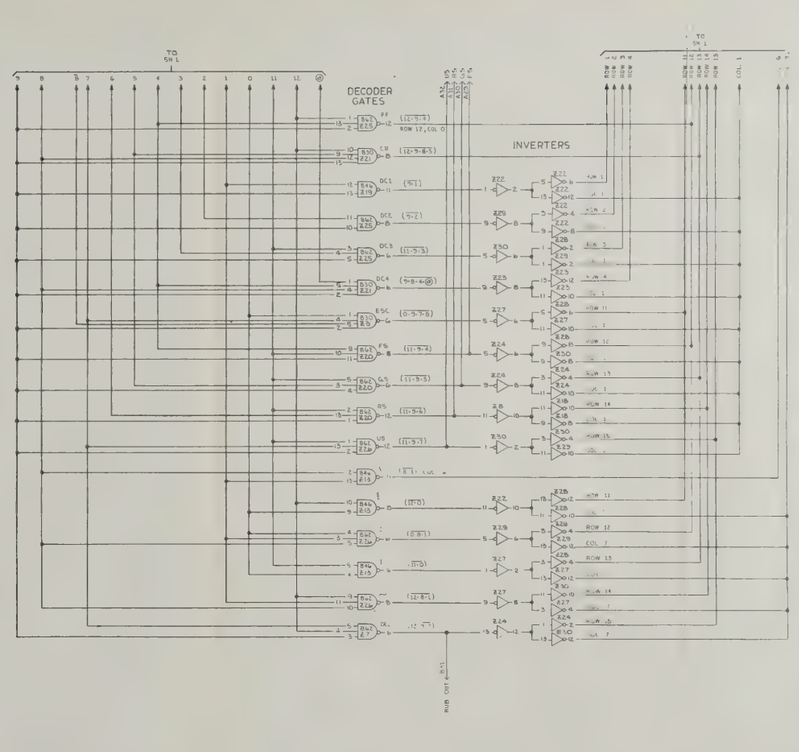


FIGURE 62
HOLL-USASCII, 85 CHAR #1 W/SHIFT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

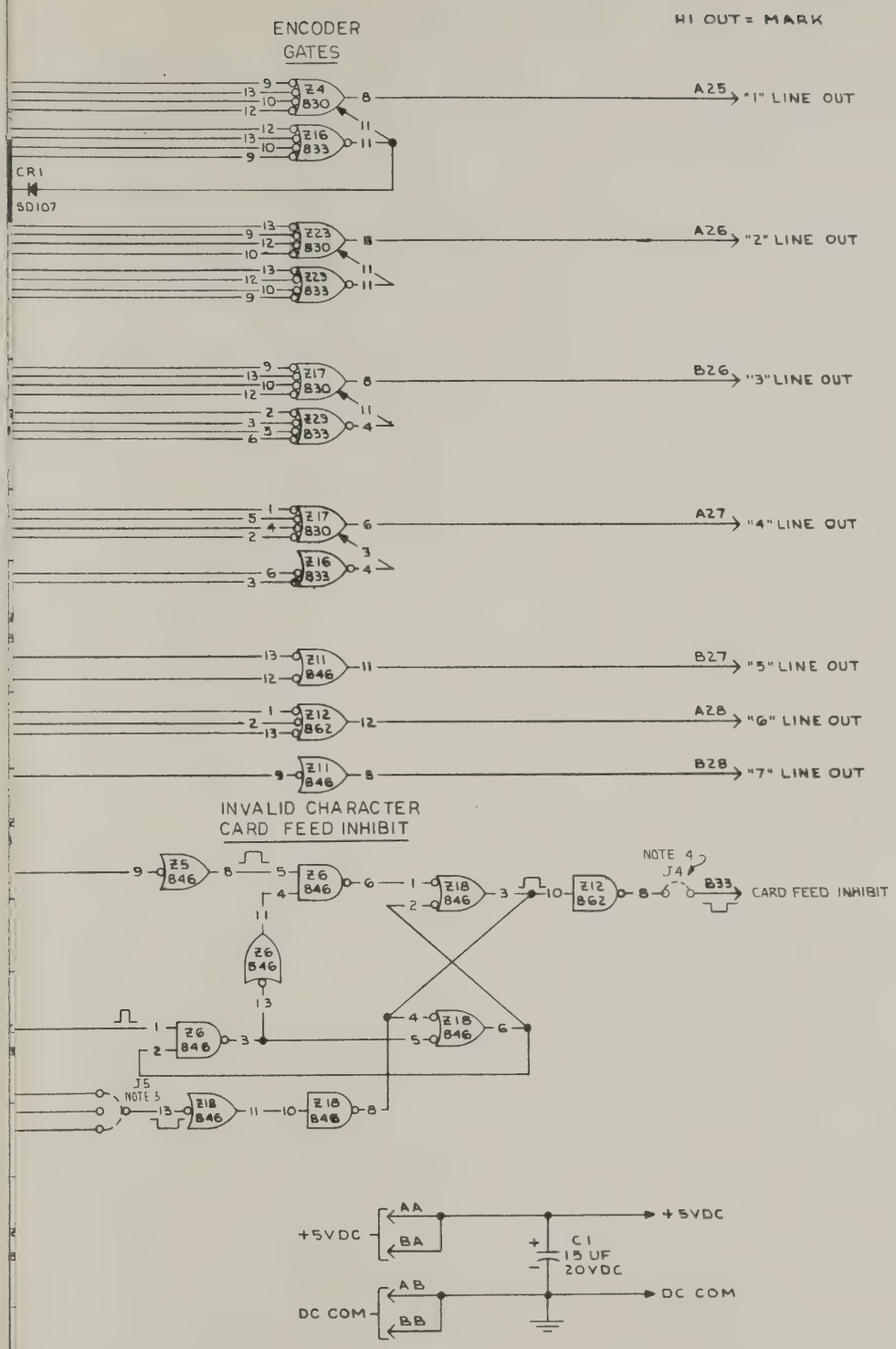
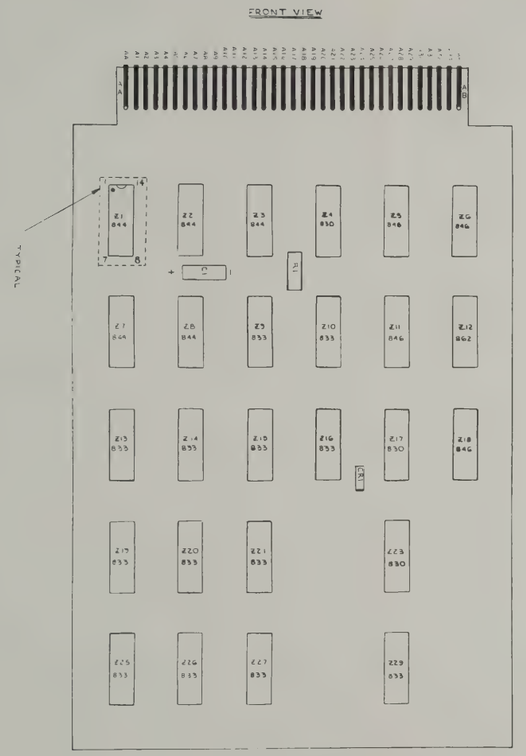
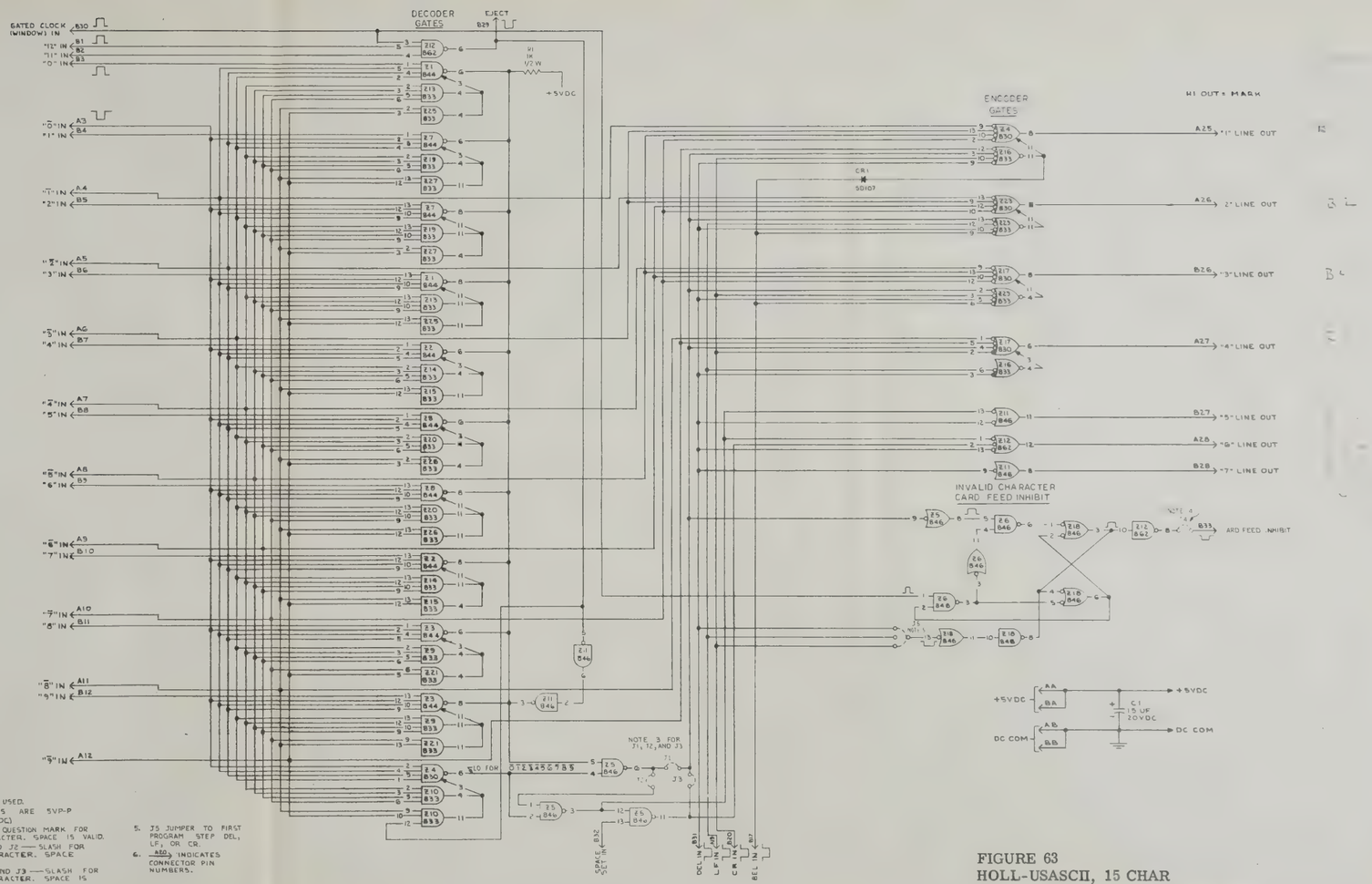


FIGURE 63
HOLL-USASCII, 15 CHAR
SCHEMATIC DIAGRAM & COMPONENT LOCATION



(DWG. NO. 01CF7869G)



NOTES:

1. POSITIVE LOGIC USED.
2. ALL WAVE FORMS ARE 5VP-P (DVDC TO +5VDC)
3. JUMPER J1 — QUESTION MARK FOR INVALID CHARACTER. SPACE IS VALID.
   JUMPERS J1 AND J2 — SLASH FOR INVALID CHARACTER. SPACE IS VALID.
   JUMPERS J2 AND J3 — SLASH FOR INVALID CHARACTER. SPACE IS NOT VALID.
4. JUMPER J4 — INHIBITS CARD FEED AFTER INVALID CHARACTER.
5. J5 JUMPER TO FIRST PROGRAM STEP DEL, LF, OR CR.
6. ⟨A6⟩ INDICATES CONNECTOR PIN NUMBERS.

(DWG. NO. 63DF7869G)

FIGURE 63
HOLL-USASCII, 15 CHAR
SCHEMATIC DIAGRAM & COMPONENT LOCATION

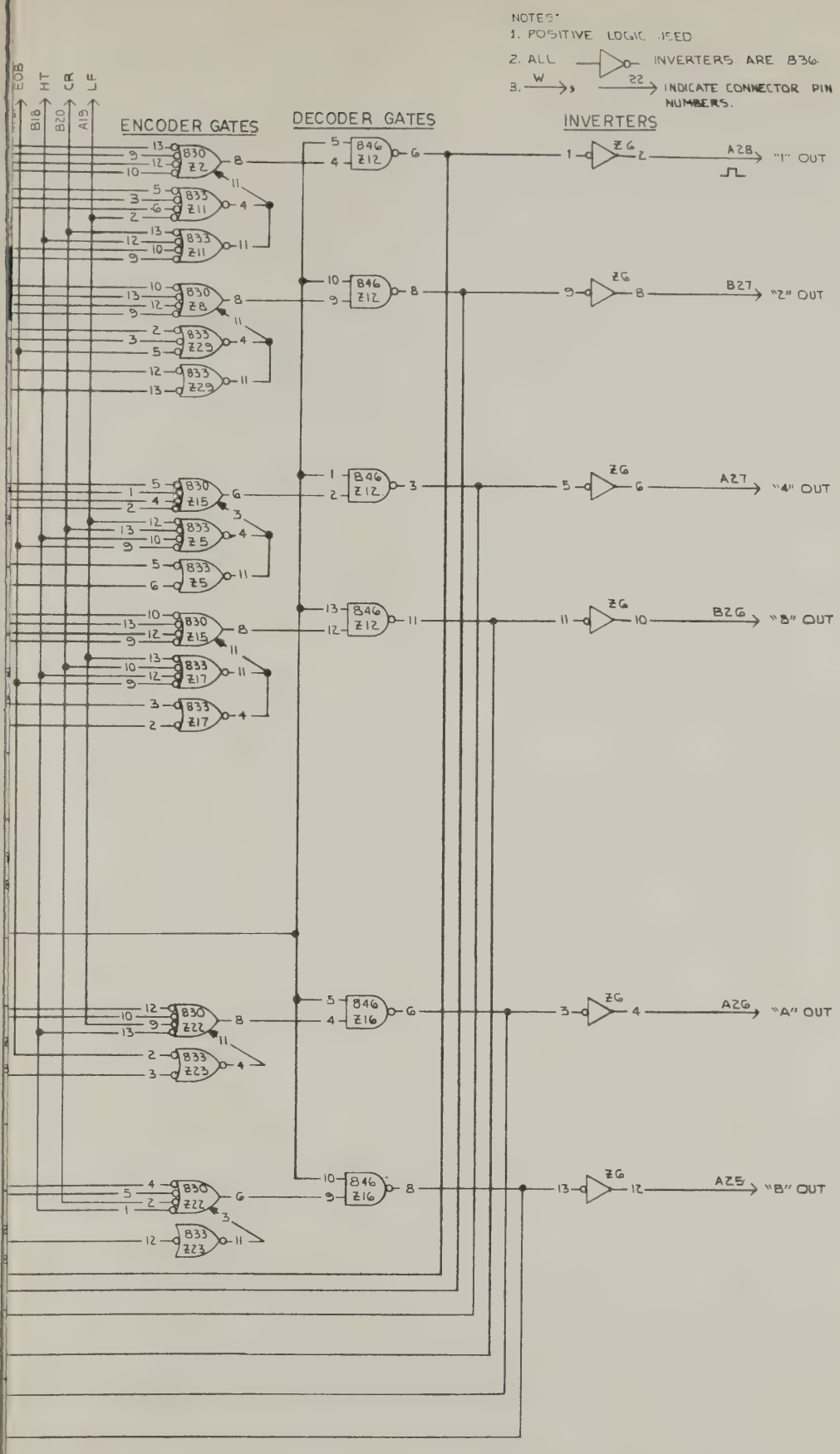
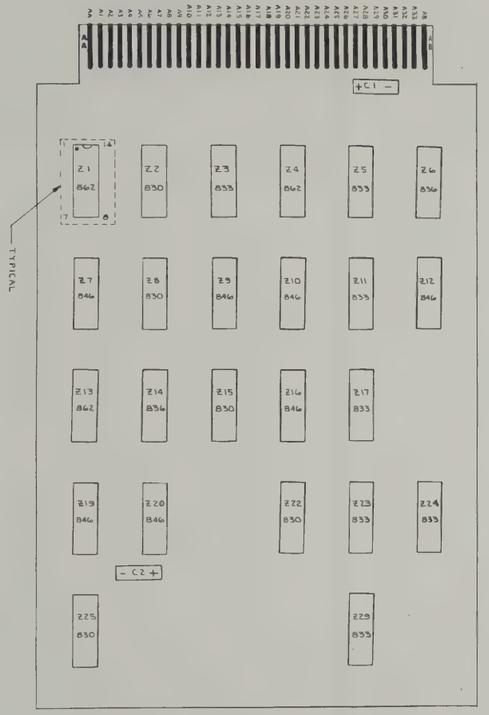
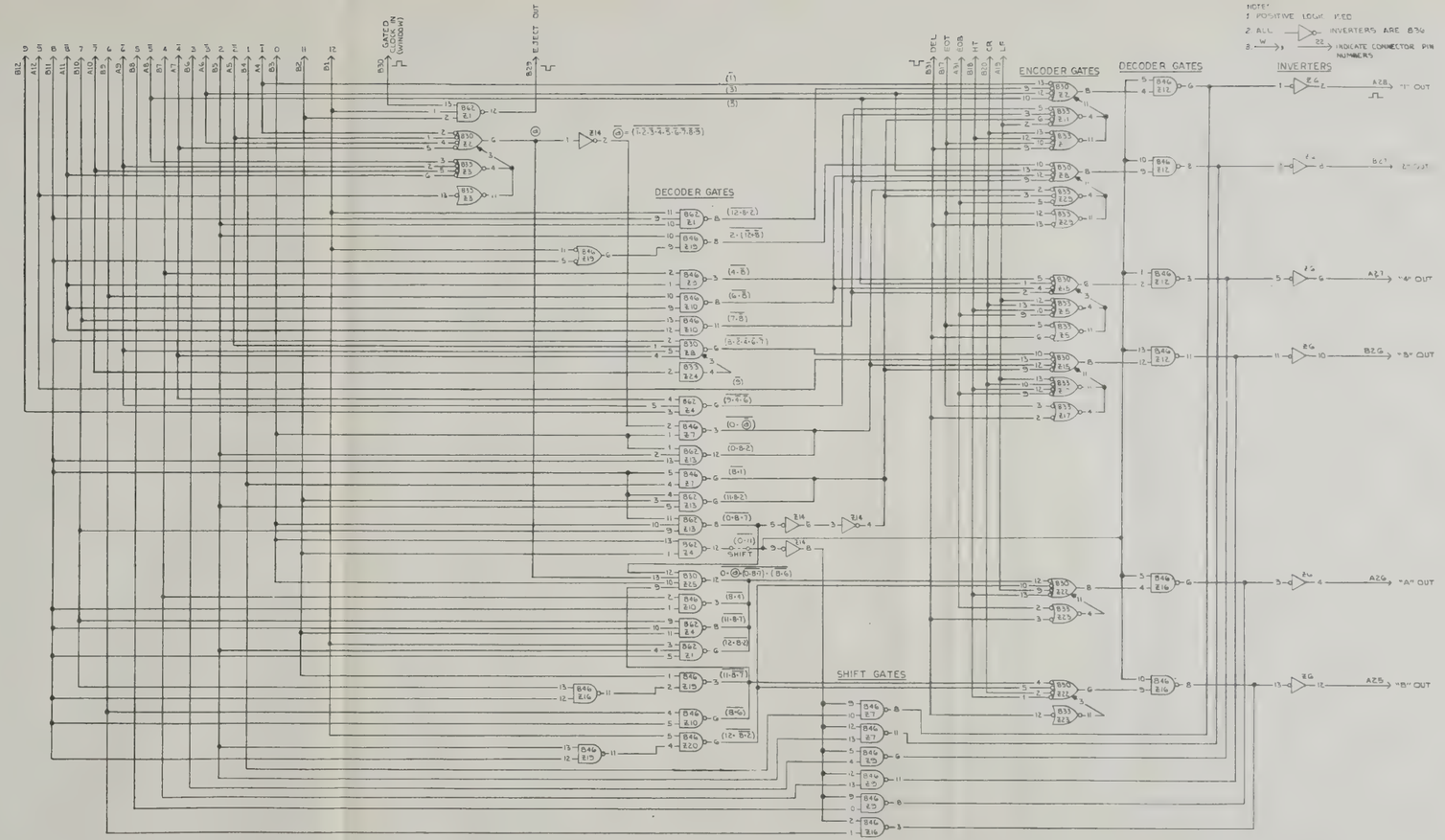
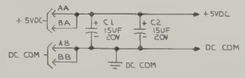


FIGURE 64
HOLL-PTTC/BCD, 64 CHAR W/SHIFT
SCHEMATIC DIAGRAM & COMPONENT LOCATION



(DWG. NO. 01CF7784G)





DWG. NO. 63DF7784G)

FIGURE 64
HOLL-PTTC/BCD, 64 CHAR W/SHIFT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

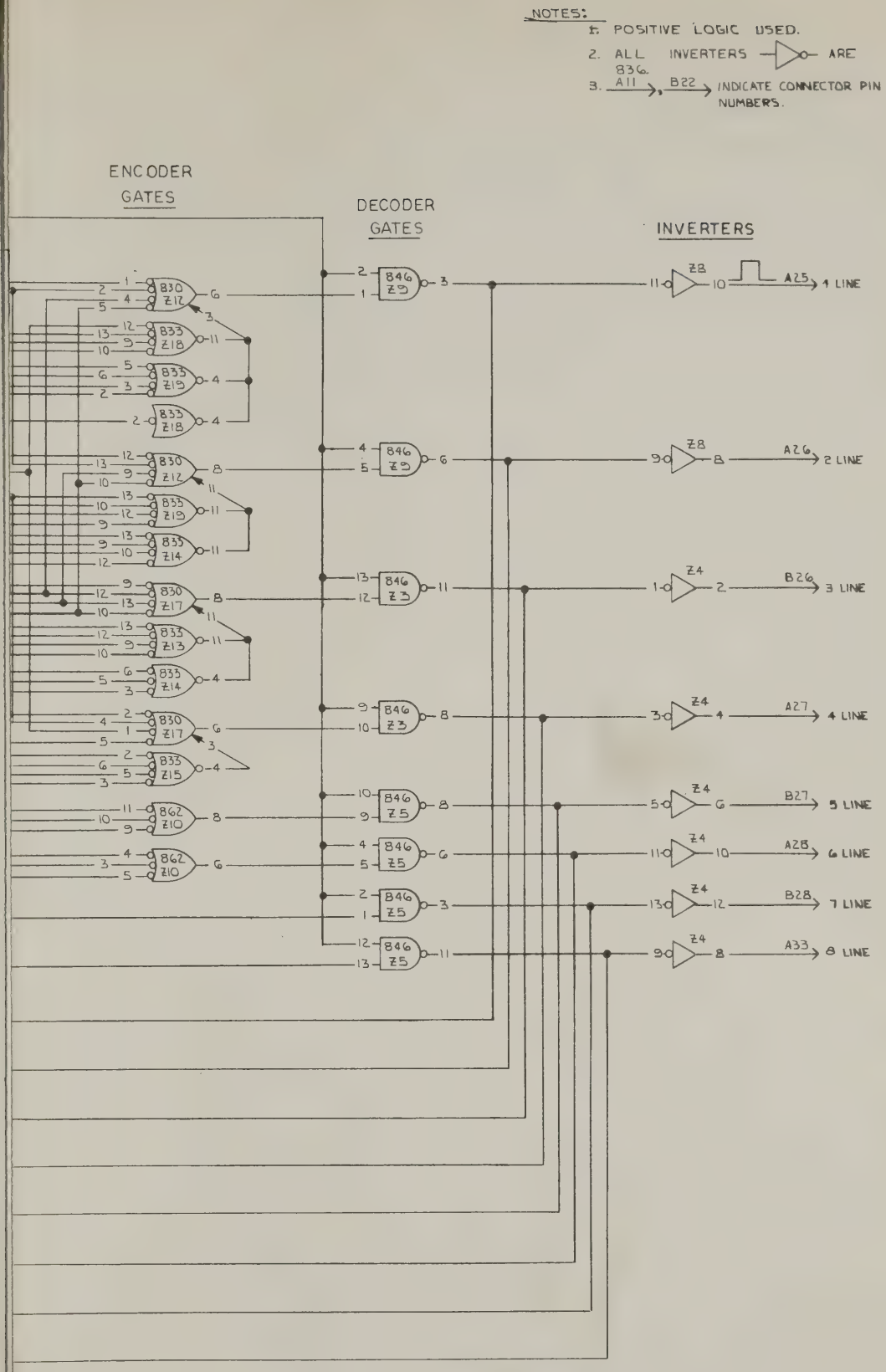
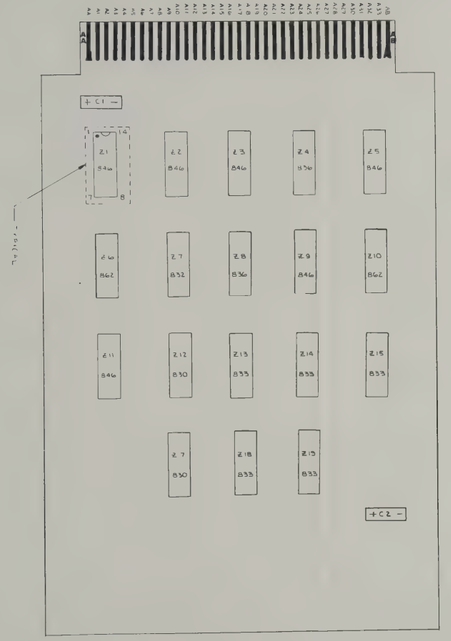
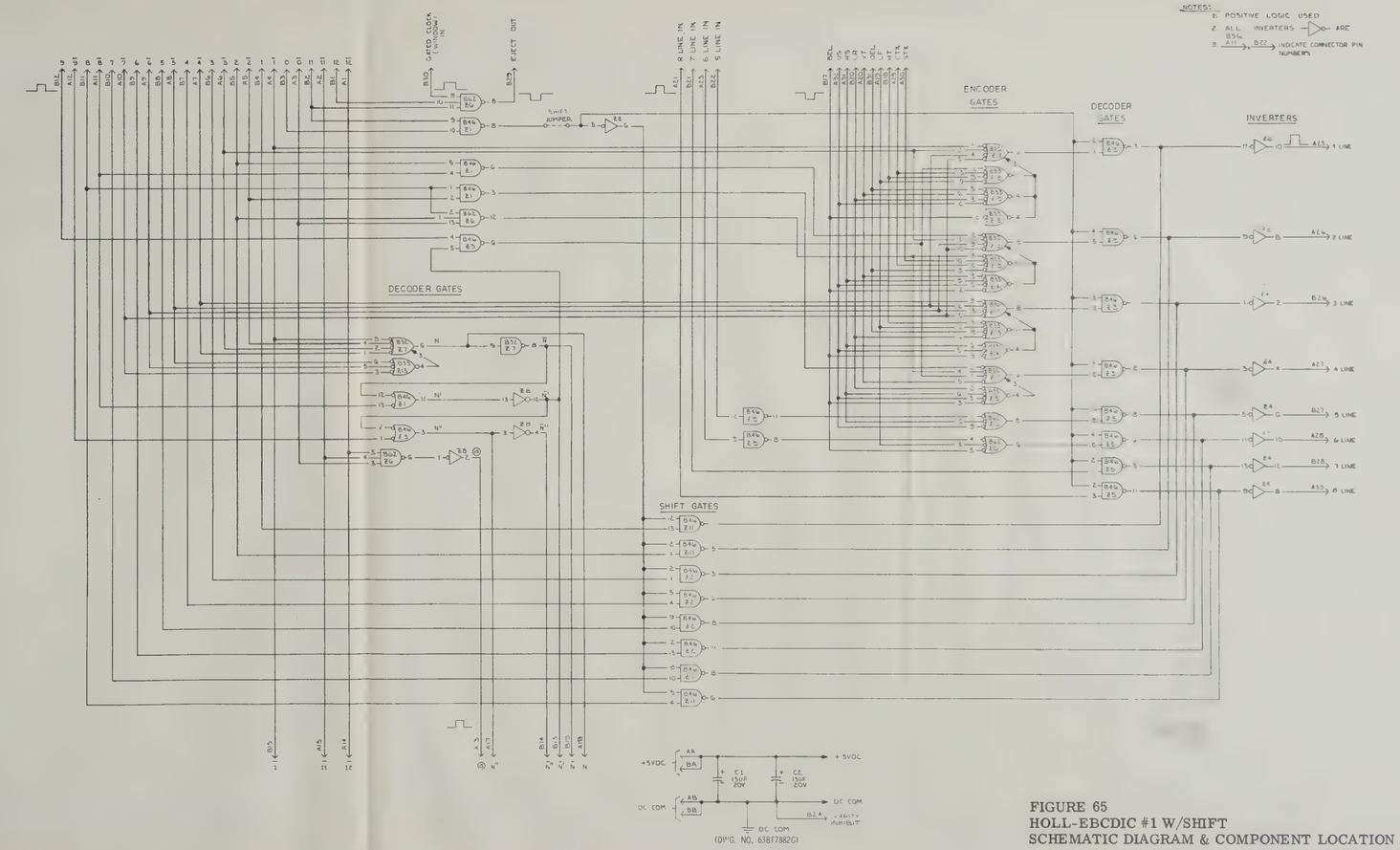


FIGURE 65
HOLL-EBCDIC #1 W/SHIFT
SCHEMATIC DIAGRAM & COMPONENT LOCATION



(DWG. NO. 01CF7882G)



(DWG. NO. 63BF7882G)

FIGURE 65
HOLL-EBCDIC #1 W/SHIFT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

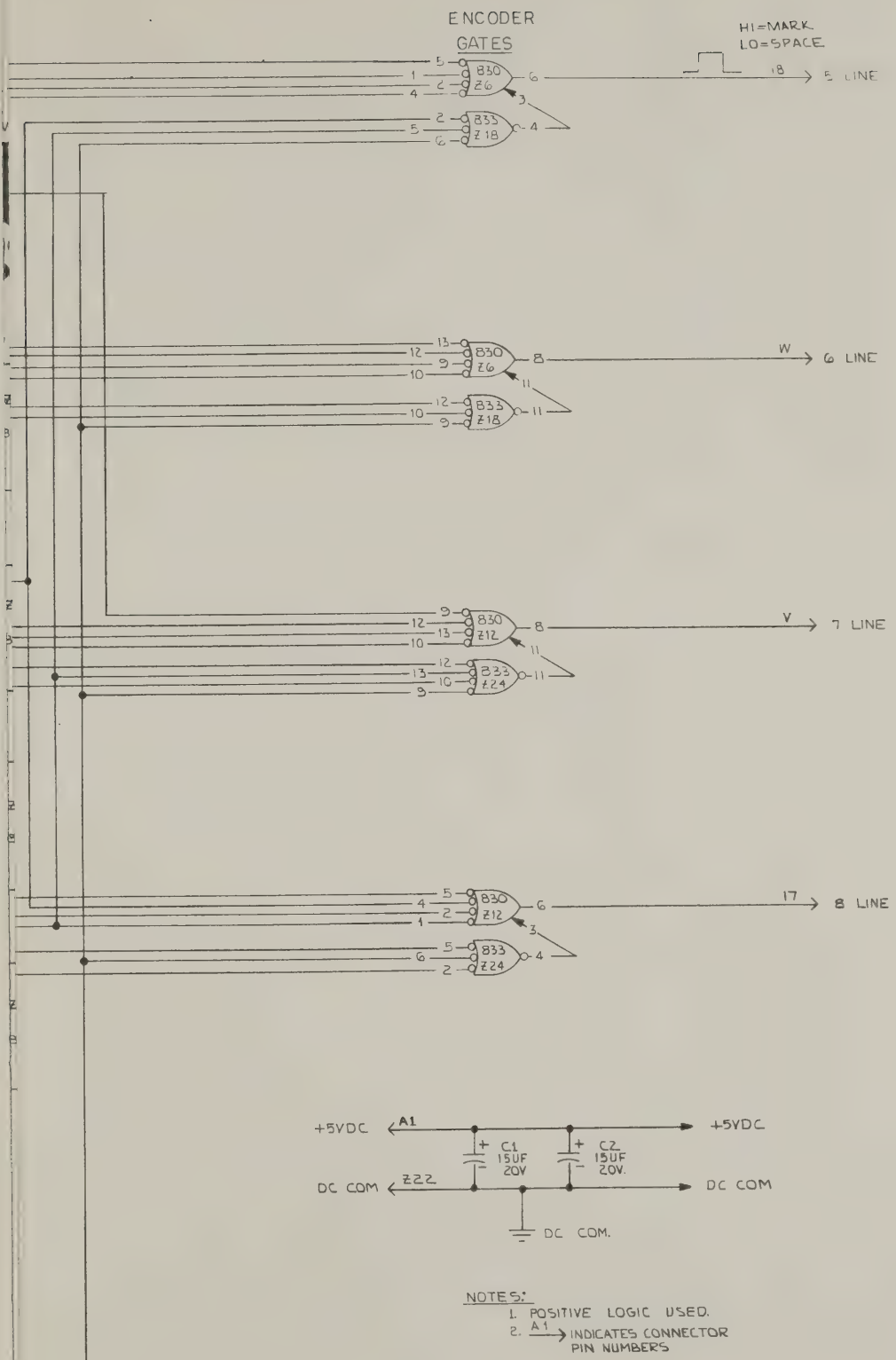
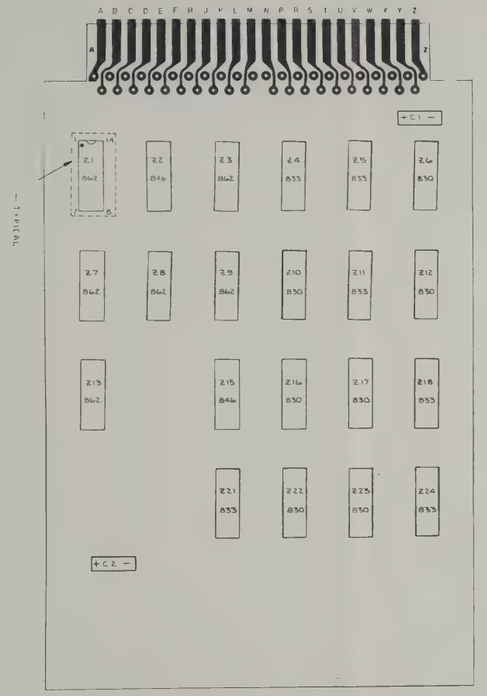
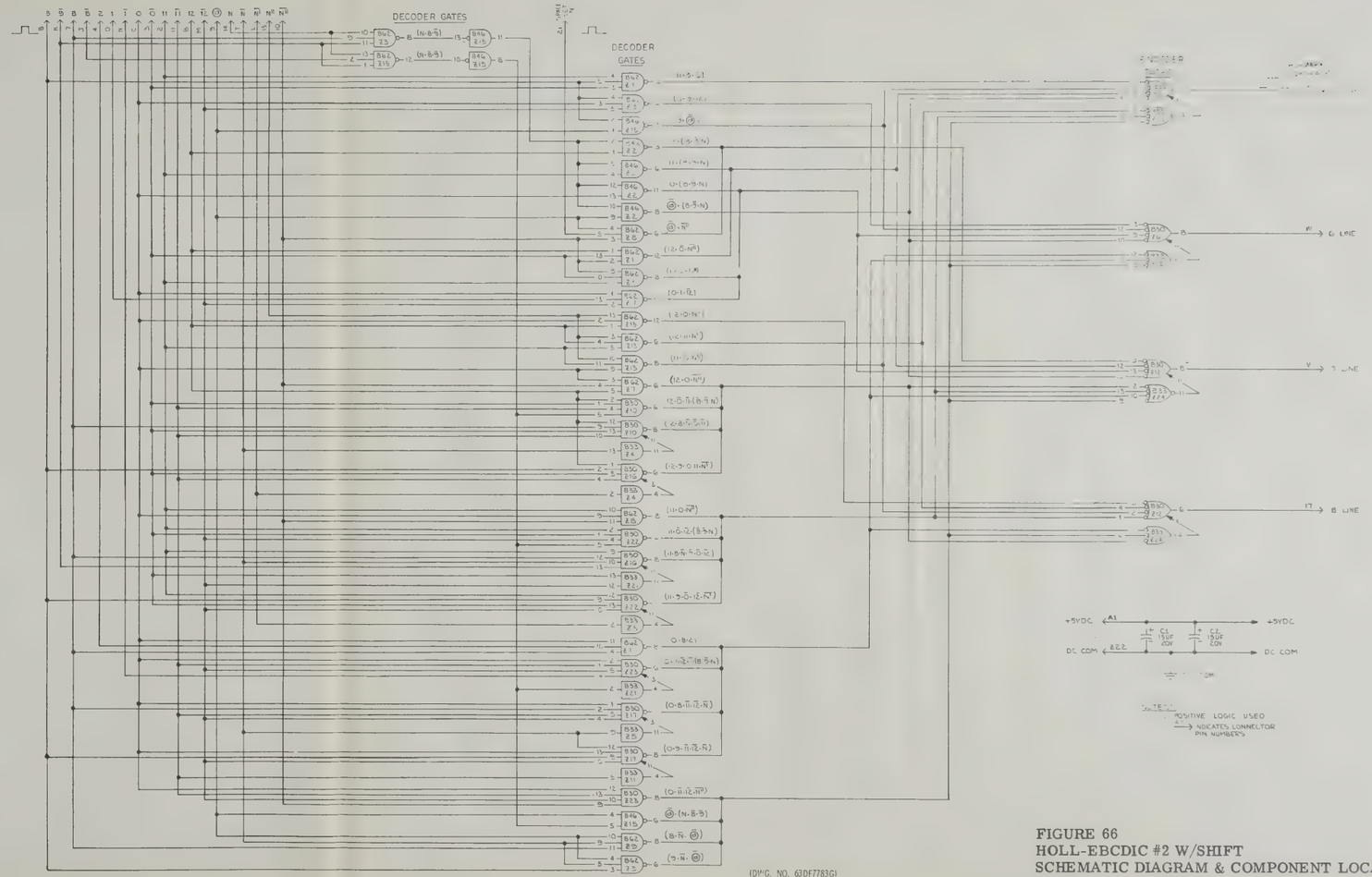


FIGURE 66
HOLL-EBCDIC #2 W/SHIFT
SCHEMATIC DIAGRAM & COMPONENT LOCATION



(DWG. NO. 01CF7783G)



(DWG. NO. 63DF7783G)

FIGURE 66
HOLL-EBCDIC #2 W/SHIFT
SCHEMATIC DIAGRAM & COMPONENT LOCATION

NOTES:
1. POSITIVE LOGIC USED.
2. A25 →, B1 → INDICATE CONNECTOR PIN NUMBERS.

" OUT

5" OUT

4" OUT

3" OUT

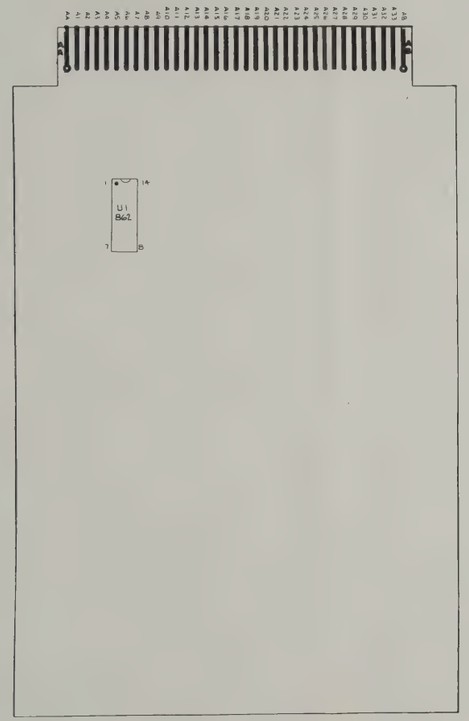
2" OUT

7" OUT

8" OUT

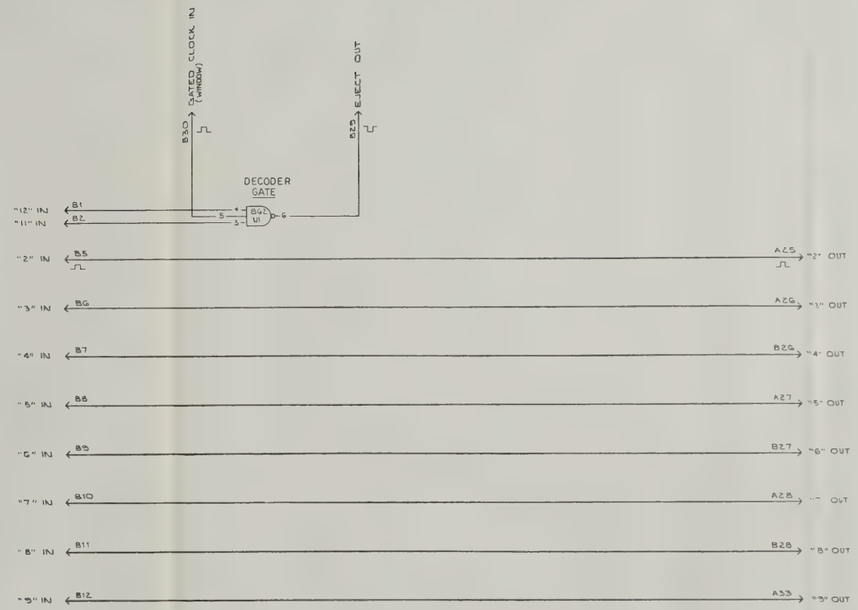
3" OUT

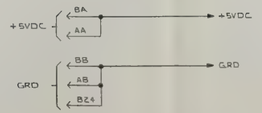
FIGURE 67
HOLL-HOLL (12 BIT PARALLEL)
SCHEMATIC DIAGRAM & COMPONENT LOCATION



(DWG. NO. 01CF7785G)

NOTES:
1. POSITIVE LOGIC USED
2. A25, B1 → INDICATE CONNECTOR PIN NUMBERS.


B30 GATED CLOCK IN (WINDOW)
B25 EJECT OUT
DECODER GATE
B&Z U1
"12" IN B1
"11" IN B2
"2" IN B5 A25 "2" OUT
"3" IN B6 A26 "3" OUT
"4" IN B7 B26 "4" OUT
"5" IN B8 A27 "5" OUT
"6" IN B9 B27 "6" OUT
"7" IN B10 A28 "7" OUT
"8" IN B11 B28 "8" OUT
"9" IN B12 A33 "9" OUT



(DWG. NO. 63DF7785G)

FIGURE 67
HOLL-HOLL (12 BIT PARALLEL)
SCHEMATIC DIAGRAM & COMPONENT LOCATION

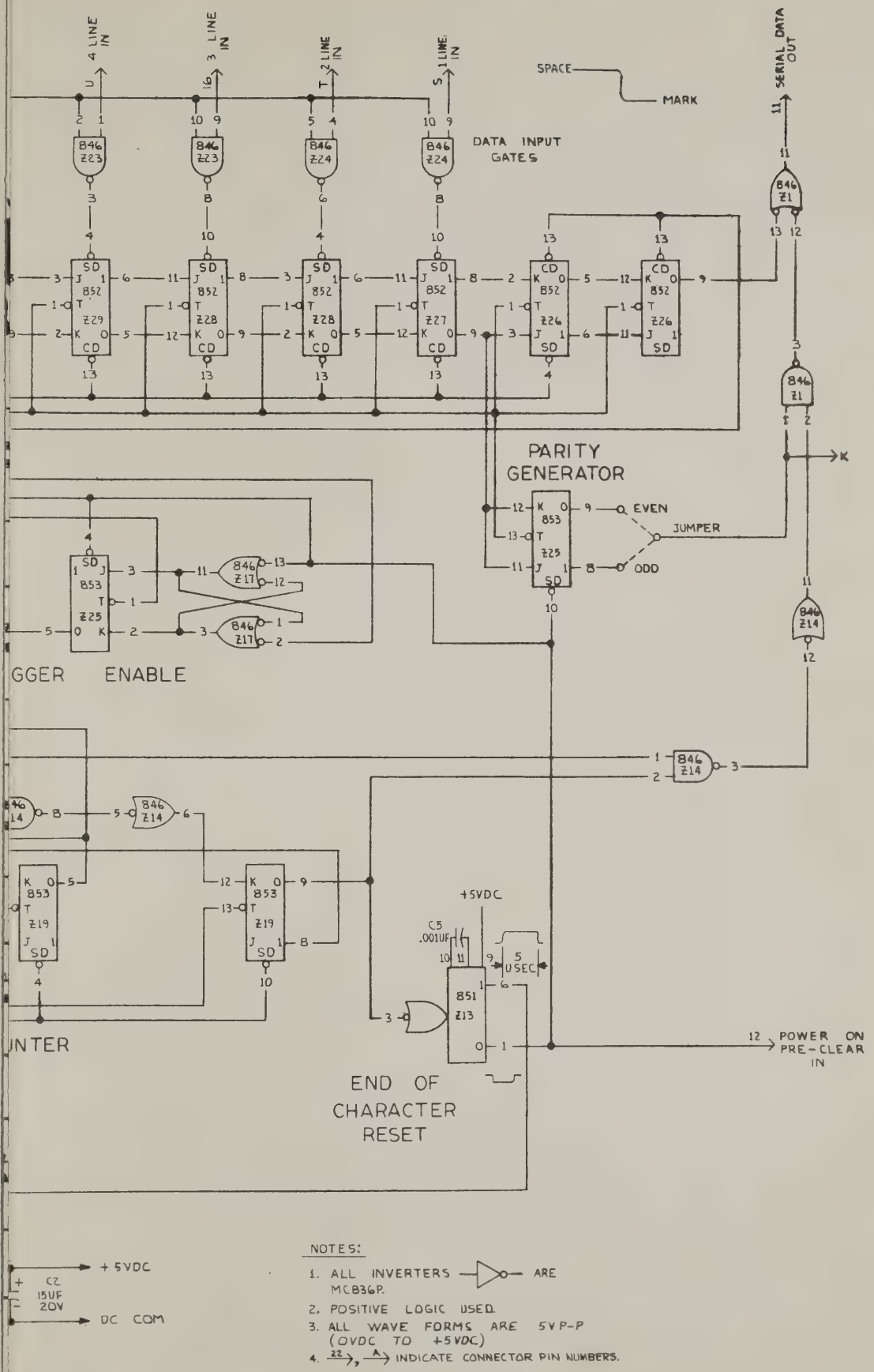
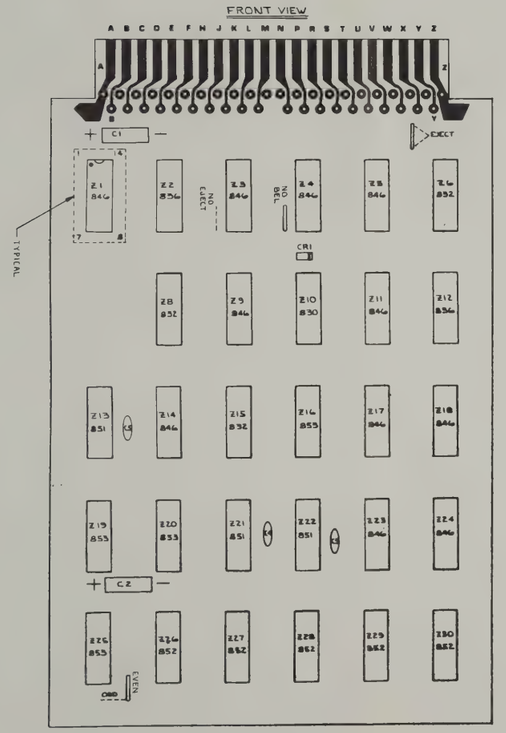
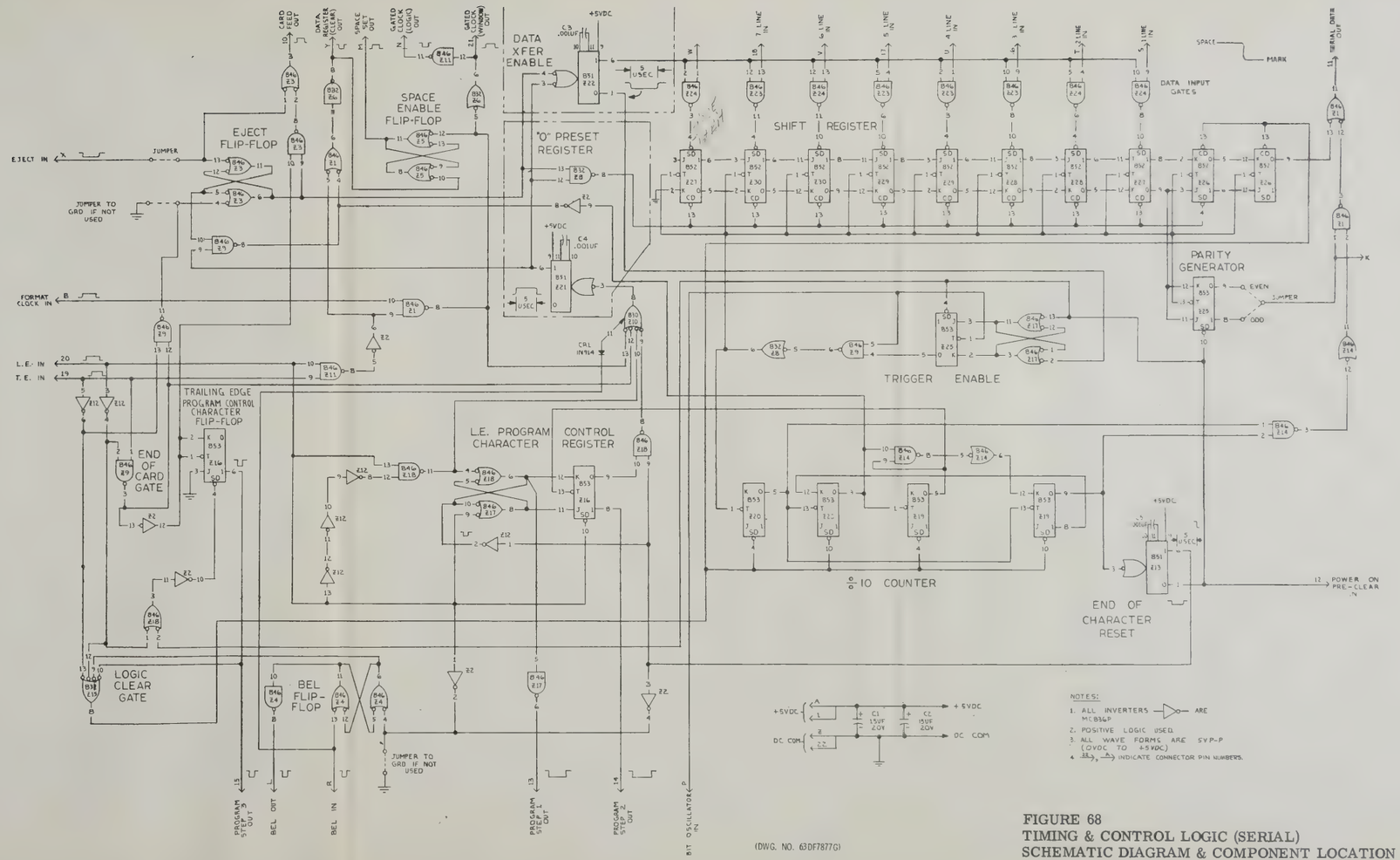


FIGURE 68
TIMING & CONTROL LOGIC (SERIAL)
SCHEMATIC DIAGRAM & COMPONENT LOCATION



(DWG. NO. 01CF7877G)



(DWG. NO. 63DF7877G)

FIGURE 68
TIMING & CONTROL LOGIC (SERIAL)
SCHEMATIC DIAGRAM & COMPONENT LOCATION

NOTES:

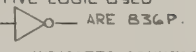
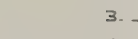
1. POSITIVE LOGIC USED
2. ALL  ARE 836P.
3.  INDICATES CONNECTOR PIN NUMBER.
4. TABLE 1 DENOTES THE SIGNAL NOMENCLATURE ON THE DATA INPUT LINES FOR THE VARIOUS INPUT LANGUAGES AVAILABLE.

TABLE 1 DATA INPUT LINES

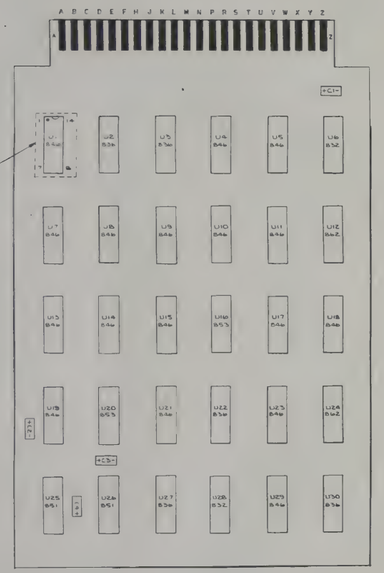
DATA INPUT PINS	LANGUAGE			
	USASC II	HOLLERITH	PTTC/BCD	EBCDIC
W	N.A.	9 LINE	N.A.	8 LINE
18	7 LINE	8 LINE	N.A.	7 LINE
V	6 LINE	7 LINE	1 LINE	6 LINE
17	5 LINE	6 LINE	2 LINE	5 LINE
U	4 LINE	5 LINE	4 LINE	4 LINE
16	3 LINE	4 LINE	8 LINE	3 LINE
T	2 LINE	3 LINE	A LINE	2 LINE
S	1 LINE	2 LINE	B LINE	1 LINE
5	N.A	1 LINE	N.A.	N.A.
4	N.A.	0 LINE	N.A.	N.A.
3	N.A.	11 LINE	N.A.	N.A.
2	N.A.	12 LINE	N.A.	N.A.

5. TABLE 2 DENOTES THE SIGNAL NOMENCLATURE ON THE DATA OUTPUT LINES FOR THE VARIOUS INPUT LANGUAGES AVAILABLE.

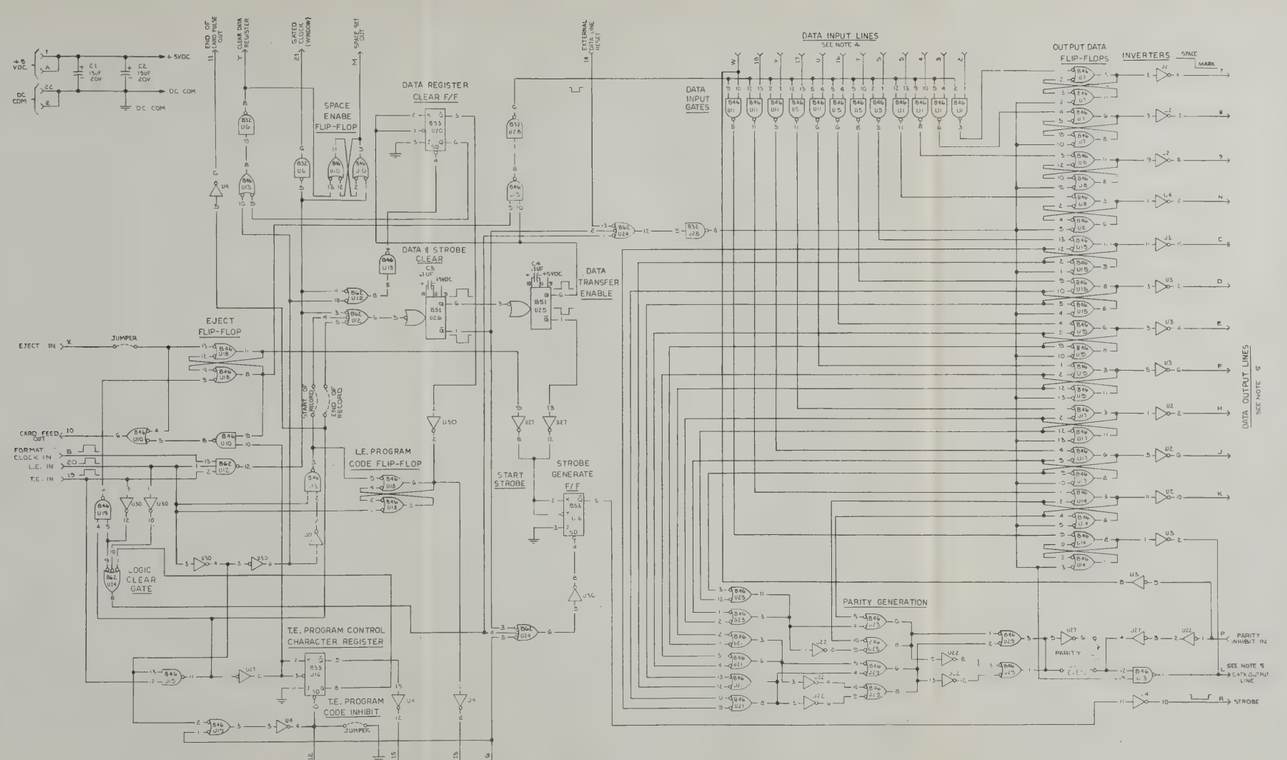
TABLE 2 DATA OUTPUT LINES

DATA OUTPUT PIN	LANGUAGE			
	USASC II	HOLLERITH	PTTC/BCD	EBCDIC
7	N.A.	12 LINE	N.A.	N.A.
8	N.A.	11 LINE	N.A.	N.A.
9	N.A.	0 LINE	N.A.	N.A.
N	N.A.	1 LINE	N.A.	N.A.
C	1 LINE	2 LINE	B LINE	1 LINE
D	2 LINE	3 LINE	A LINE	2 LINE
E	3 LINE	4 LINE	8 LINE	3 LINE
F	4 LINE	5 LINE	4 LINE	4 LINE
H	5 LINE	6 LINE	2 LINE	5 LINE
J	6 LINE	7 LINE	1 LINE	6 LINE
K	7 LINE	8 LINE	W.A	7 LINE
L	PARITY	9 LINE	PARITY	8 LINE

FIGURE 69
TIMING & CONTROL LOGIC (PARALLEL)
SCHEMATIC DIAGRAM & COMPONENT LOCATION



(DWG. NO. 63DF7786C)



(DWG. NO. 63DF7786G)

[illegible] INDICATES CONNECTOR PIN NUMBER

TABLE 1 DENOTES THE SIGNAL NOMENCLATURE ON THE DATA INPUT LINES FOR THE VARIOUS INPUT LANGUAGES AVAILABLE

*TABLE 1 DATA INPUT LINES

DATA INPUT PINS	LANGUAGE			
	USASCII	HOLLERITH	PTTC/FIELD	EBCDIC
W	N.A.	9 LINE	N.A.	8 LINE
B	7 LINE	8 LINE	N.A.	7 LINE
Y	6 LINE	7 LINE	9 LINE	6 LINE
11	5 LINE	6 LINE	8 LINE	5 LINE
J	4 LINE	5 LINE	4 LINE	4 LINE
16	3 LINE	4 LINE	3 LINE	3 LINE
T	2 LINE	3 LINE	2 LINE	2 LINE
S	1 LINE	2 LINE	1 LINE	1 LINE
5	N.A.	1 LINE	N.A.	N.A.
4	N.A.	0 LINE	N.A.	N.A.
3	N.A.	11 LINE	N.A.	N.A.
2	N.A.	12 LINE	N.A.	N.A.

*TABLE 2 DENOTES THE SIGNAL NOMENCLATURE ON THE DATA OUTPUT LINES FOR THE VARIOUS INPUT LANGUAGES AVAILABLE

*TABLE 2 DATA OUTPUT LINES

DATA OUTPUT PIN	LANGUAGE			
	USASCII	HOLLERITH	PTTC/8-2	EBCDIC
7	N.A.	12 LINE	N.A.	N.A.
8	N.A.	11 LINE	N.A.	N.A.
9	N.A.	0 LINE	N.A.	N.A.
N	N.A.	1 LINE	N.A.	N.A.
C	1 LINE	2 LINE	8 LINE	1 LINE
D	2 LINE	3 LINE	A LINE	2 LINE
E	3 LINE	4 LINE	B LINE	3 LINE
F	4 LINE	5 LINE	4 LINE	4 LINE
H	5 LINE	6 LINE	2 LINE	5 LINE
J	6 LINE	7 LINE	1 LINE	6 LINE
K	7 LINE	8 LINE	9A	7 LINE
L	PARITY	9 LINE	PARITY	8 LINE

FIGURE 69
TIMING & CONTROL LOGIC (PARALLEL)
SCHEMATIC DIAGRAM & COMPONENT LOCATION

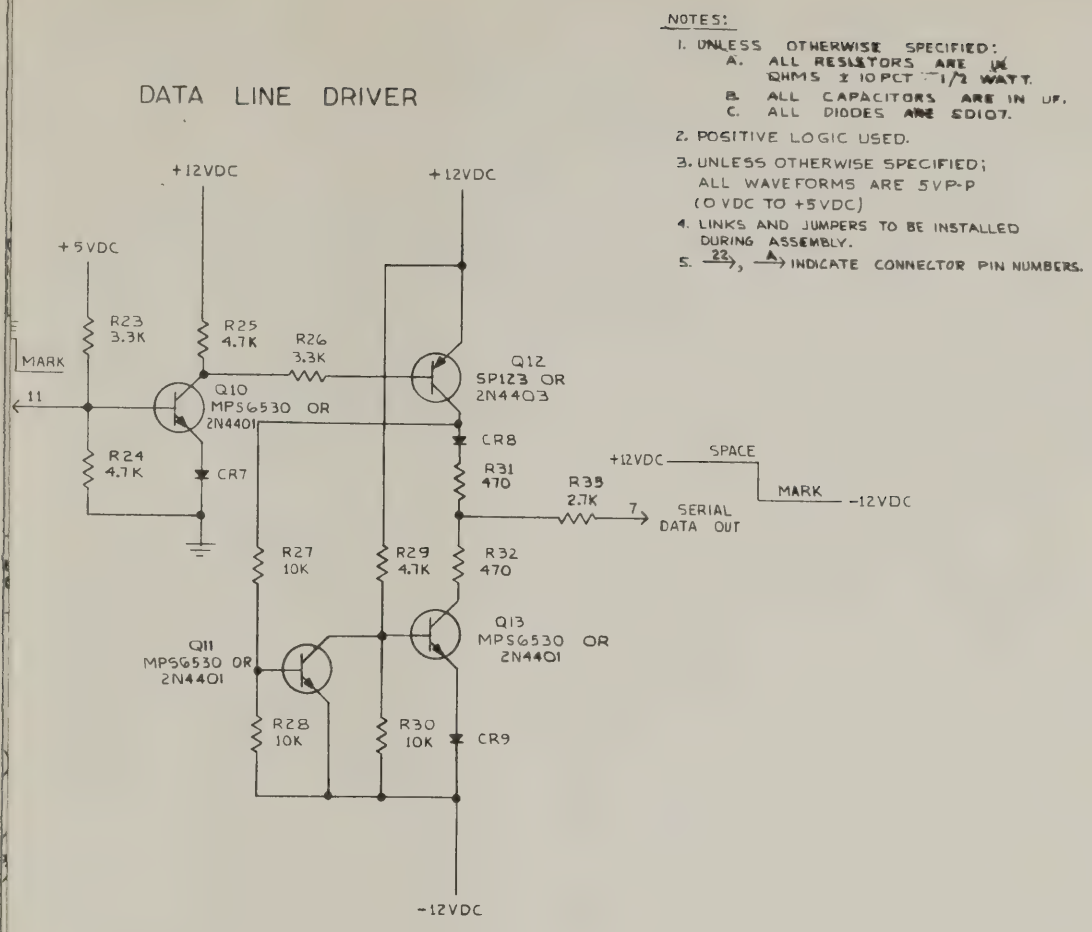
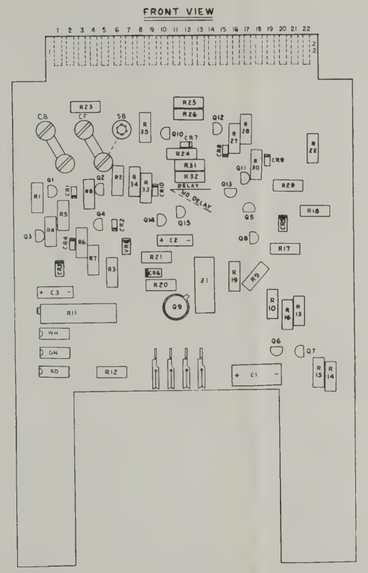
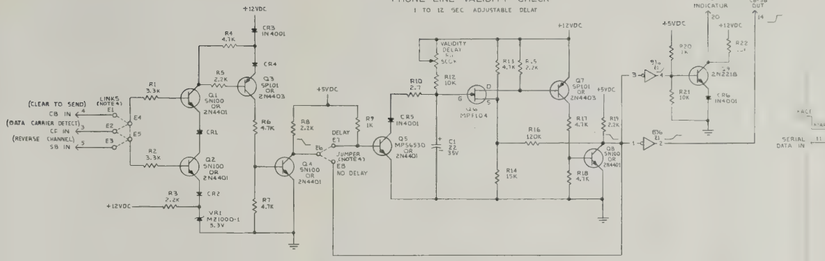
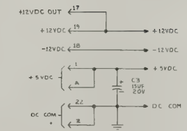


FIGURE 70
DATA OUT-PHONE
SCHEMATIC DIAGRAM & COMPONENT LOCATION



(DWG. NO. 01CF7878C)





(DWG. NO. 63DF7878G)

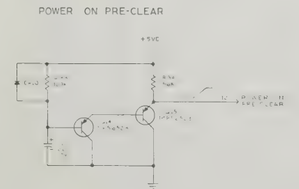
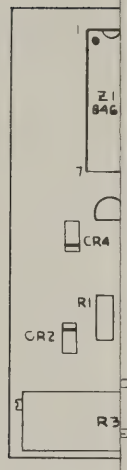


FIGURE 70
DATA OUT-PHONE
SCHEMATIC DIAGRAM & COMPONENT LOCATION



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS ±10%, 1/4 WATT.
   B. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL CAPACITORS MUST BE IN FLAT POSITION.
3. → INDICATES CONNECTOR PIN NUMBERS.

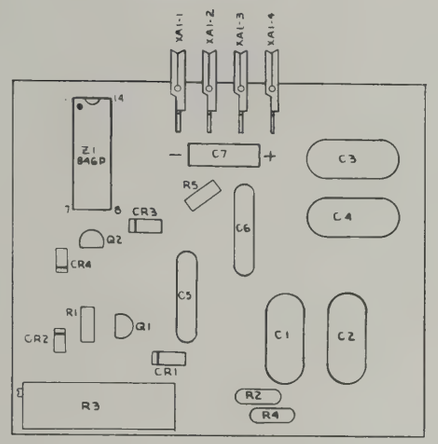
TABLE A

PART NUMBER	DESCRIPTION	C1	C2	C3	C4	C5	C6
63BF7882G01	110HZ OSC	.1	.1	.1	.1	.022	.022
63BF7882G02	1050HZ OSC		.022		.022	.01	.01

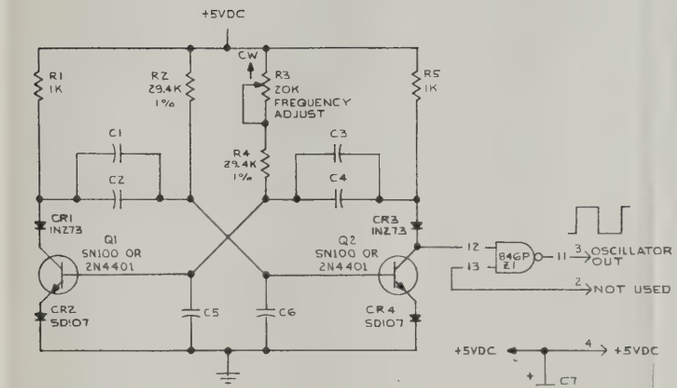
3. POSITIVE LOGIC USED
4. UNLESS OTHERWISE SPECIFIED:
   ALL WAVEFORMS ARE 5V P-P
   (0 VDC TO +5VDC)

E 71
CILLATOR
IATIC DIAGRAM & COMPONENT LOCATION

FRONT VIEW



(DWG. NO. 01CF7782G)



(DWG. NO. 63DF7782G)

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS ±10%, 1/4 WATT.
   B. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL CAPACITORS MUST BE IN FLAT POSITION.
3. (3) INDICATES CONNECTOR PIN NUMBERS.

TABLE A

PART NUMBER	DESCRIPTION	C1	C2	C3	C4	C5	C6
63BF1882G01	110HZ OSC	.1	.1	.1	.1	.022	.022
63BF1882G02	1050HZ OSC		.022		.022	.01	.01

3. POSITIVE LOGIC USED
4. UNLESS OTHERWISE SPECIFIED:
   ALL WAVEFORMS ARE 5V P-P
   (0 VDC TO +5VDC)

FIGURE 71
BIT OSCILLATOR
SCHEMATIC DIAGRAM & COMPONENT LOCATION

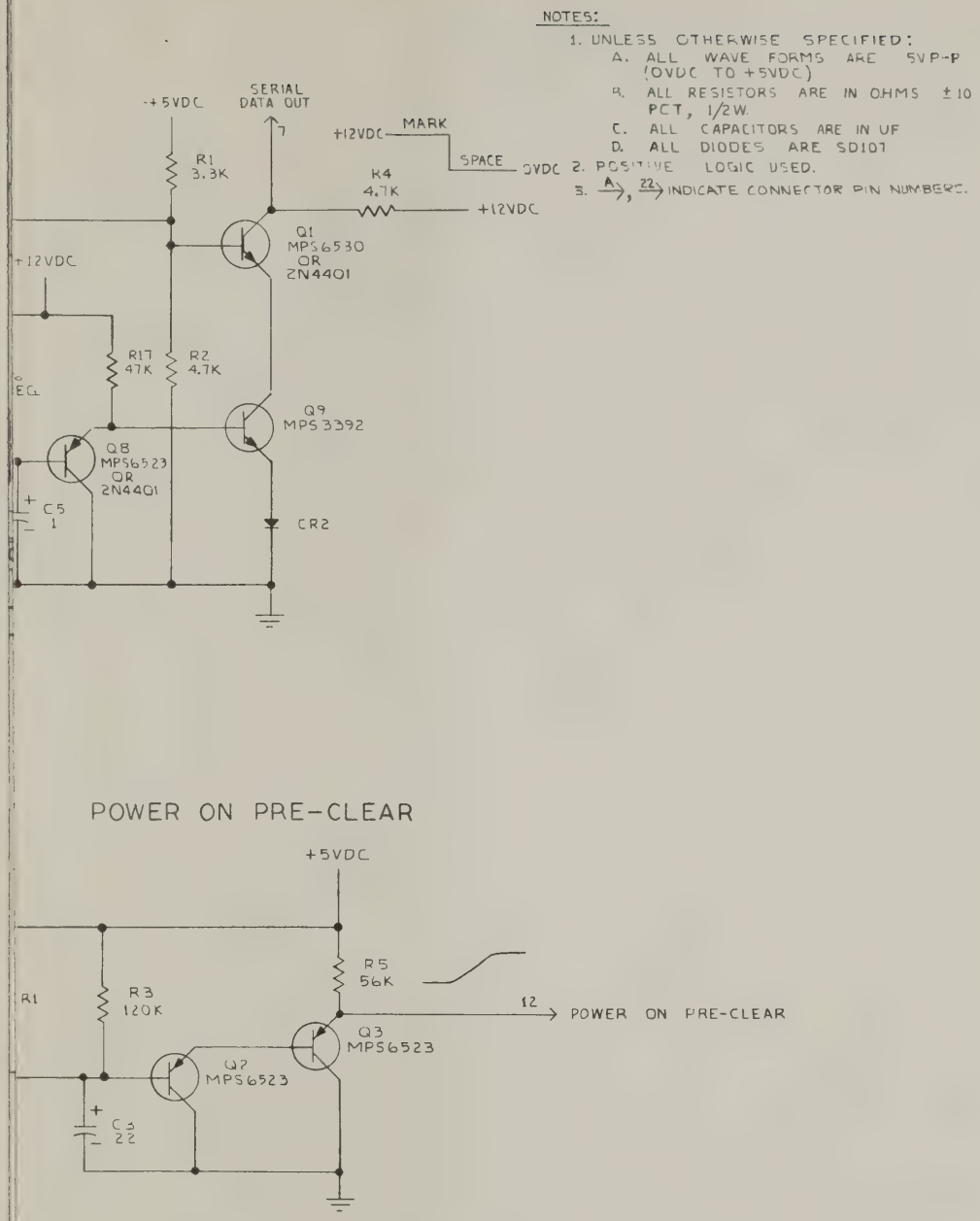
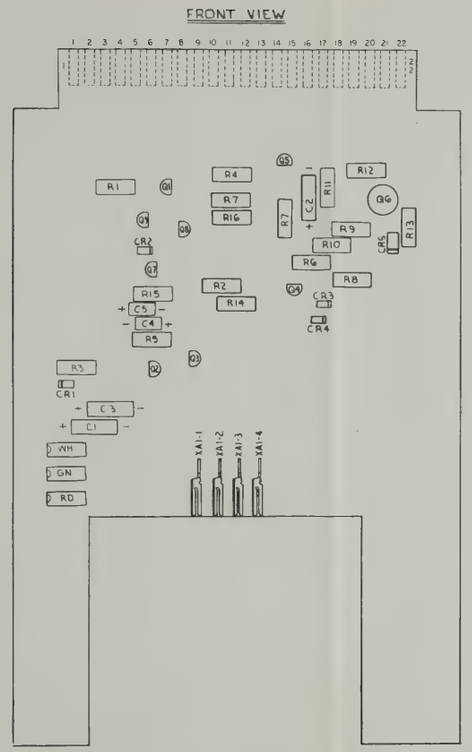
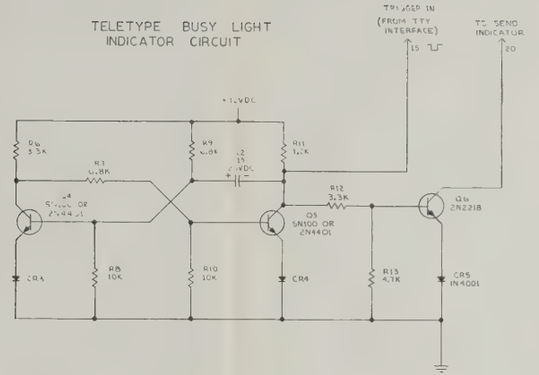
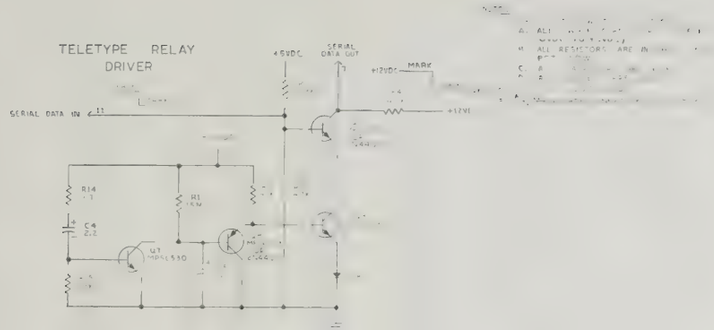


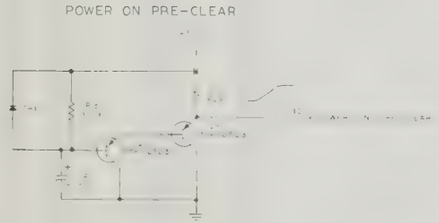
FIGURE 72
DATA OUT-TTY
SCHEMATIC DIAGRAM & COMPONENT LOCATION

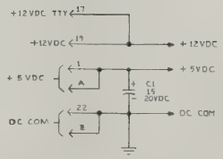


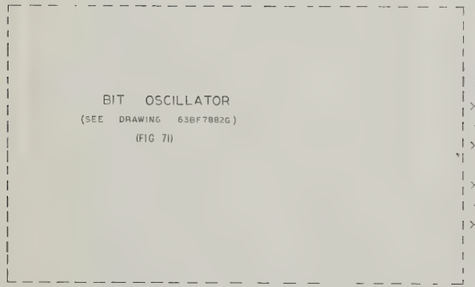
(DWG. NO. 01CF7880G)

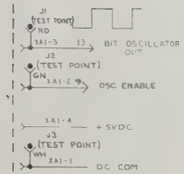








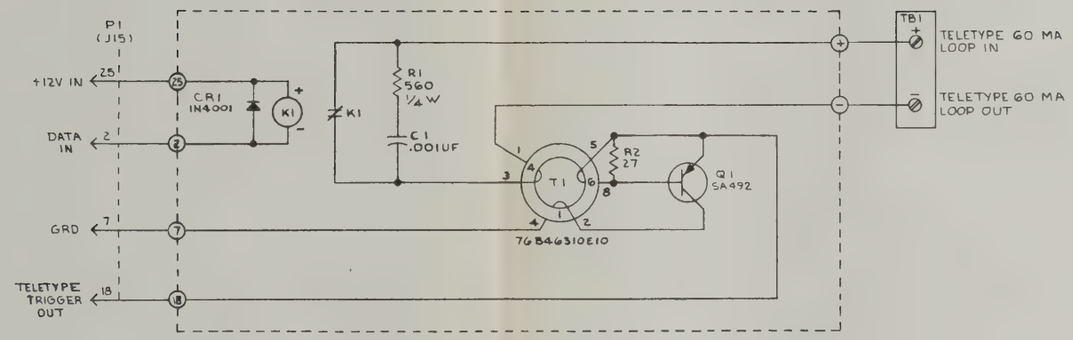




(DWG. NO. 63DF7880G)

FIGURE 72
DATA OUT-TTY
SCHEMATIC DIAGRAM & COMPONENT LOCATION

FIGURE 73
TELETYPEWRITER ADAPTOR
SCHEMATIC DIAGRAM



NOTES

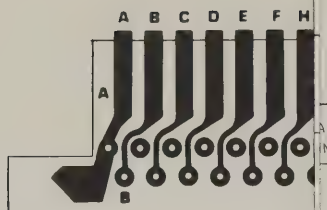
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS, ±10 PERCENT, 1/2 WATT.
2. ○ INDICATES POINTS WHERE OUTSIDE CONDUCTORS ARE CONNECTED TO PRINTED CIRCUIT BOARD.
3. K1 IS MERCURY WETTED CONTACT RELAY.
4. —2→ INDICATES CONNECTOR PIN NUMBERS.

(DWG. NO. 63BF7859G)

FIGURE 73
TELETYPEWRITER ADAPTOR
SCHEMATIC DIAGRAM

NOTES:

1. POSITIVE LOGIC USED
2. UNLESS OTHERWISE SPECIFIED:
   A. ALL CAPACITORS ARE IN UF.
   B. ALL RESISTORS ARE IN OHMS, ±10%, 1/4W
3. 18 → INDICATES CONNECTOR PIN NUMBERS.
4. TABLE 1 DENOTES THE SIGNAL NOMENCLATURE FOR THE DATA INPUT AND DATA OUTPUT LINES WITH RELATIONSHIP TO LANGUAGE USED.



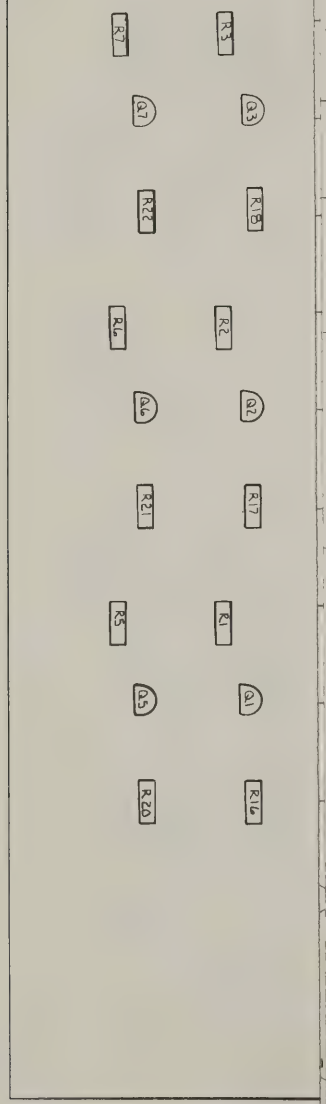


TABLE 1 DATA INPUT AND DATA OUTPUT LINES

A INPUT INS	LANGUAGE				DATA OUTPUT PINS
	USASC II	HOLLERITH	PTTC/BCD	EBCDIC	
H	N.A.	12 LINE	N.A.	N.A.	2
K	N.A.	11 LINE	N.A.	N.A.	3
M	N.A.	0 LINE	N.A.	N.A.	4
U	N.A.	1 LINE	N.A.	N.A.	5
B	1 LINE	2 LINE	B LINE	1 LINE	6
C	2 LINE	3 LINE	A LINE	2 LINE	7
D	3 LINE	4 LINE	8 LINE	3 LINE	8
F	4 LINE	5 LINE	4 LINE	4 LINE	9
J	5 LINE	6 LINE	2 LINE	5 LINE	10
L	6 LINE	7 LINE	1 LINE	6 LINE	11
N	7 LINE	8 LINE	N A	7 LINE	12
P	PARITY	9 LINE	PARTY	8 LINE	13

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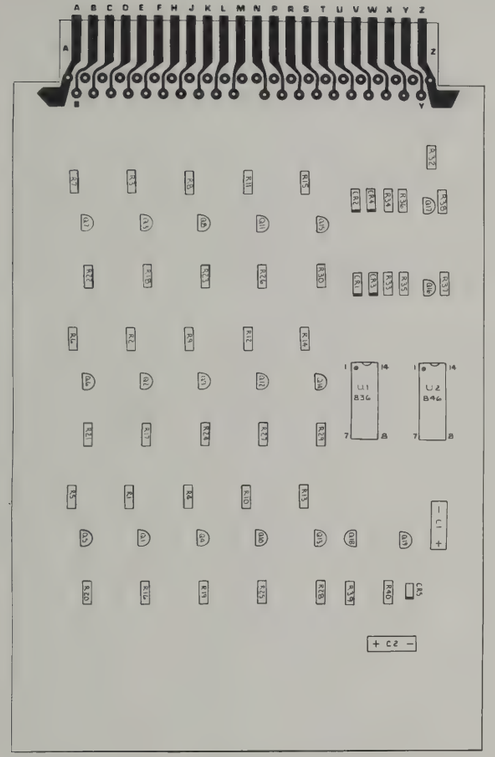
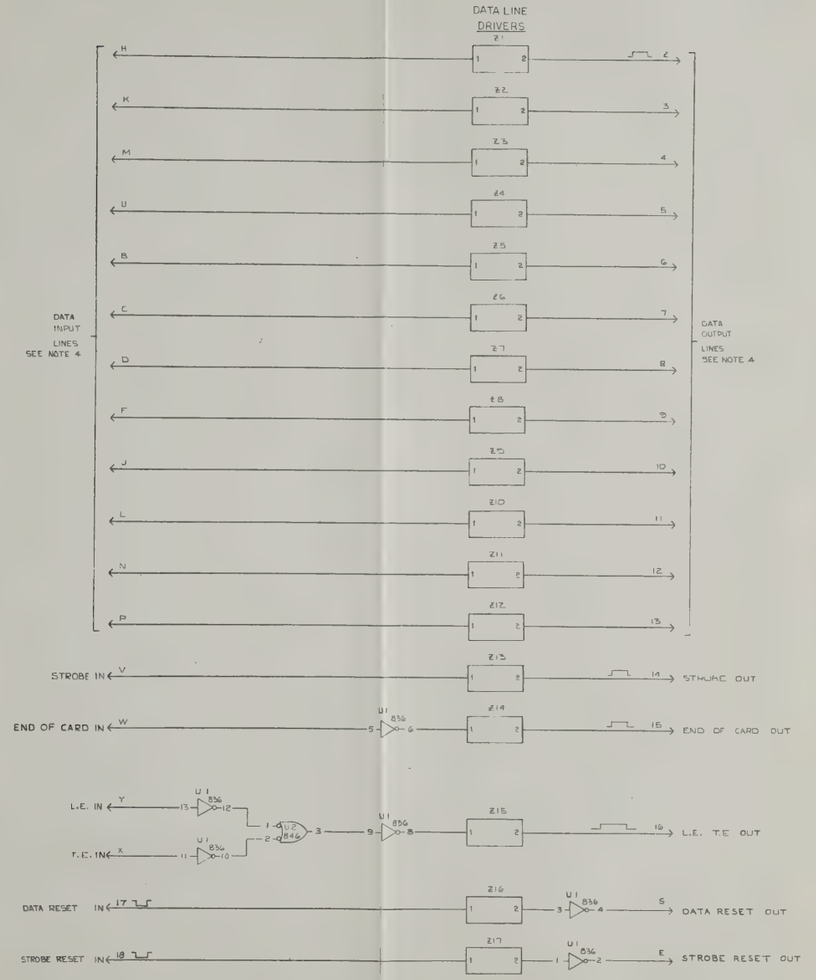
ACE DRIVER (PARALLEL)

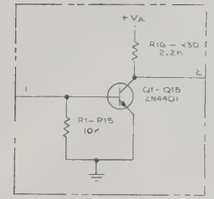
TIC DIAGRAM & COMPONENT LOCATION

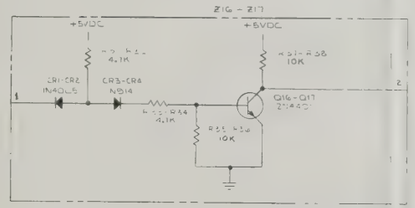


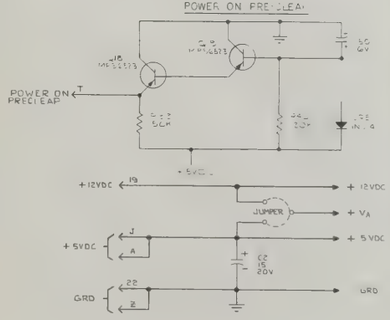
(DWG. NO. 01CF/788G)



(DWG. NO. 63D7788G)







NOTES:
1. ALL LOGIC USED
B. ALL RESISTORS ARE
2 → INDICATES CONNECTOR PIN NUMBERS
4. TABLE 1 DENOTES THE SIGNAL NOMENCLATURE FOR THE DATA INPUT AND DATA OUTPUT LINES WITH RELATIONSHIP TO LANGUAGE USED.

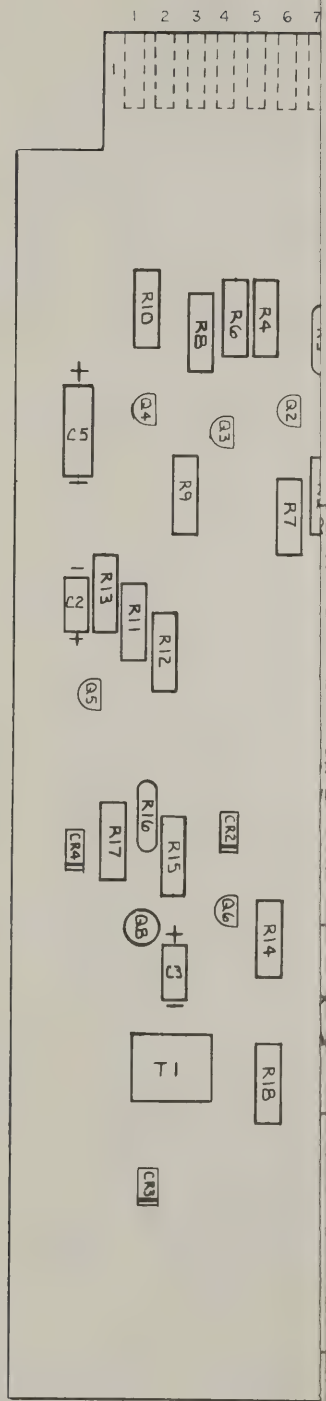
TABLE 1 DATA INPUT AND DATA OUTPUT LINES

DATA INPUT PINS	LANGUAGE				DATA OUTPUT PINS
	USASC II	HOLLERITH	PTTC/BCD	EBCDIC	
H	N.A.	12 LINE	N.A.	N.A.	2
K	N.A.	11 LINE	N.A.	N.A.	3
M	N.A.	0 LINE	N.A.	N.A.	4
U	N.A.	1 LINE	N.A.	N.A.	5
B	1 LINE	2 LINE	B LINE	1 LINE	6
C	2 LINE	3 LINE	A LINE	2 LINE	7
D	3 LINE	4 LINE	8 LINE	3 LINE	8
F	4 LINE	5 LINE	4 LINE	4 LINE	9
J	5 LINE	6 LINE	2 LINE	5 LINE	10
L	6 LINE	7 LINE	1 LINE	6 LINE	11
N	7 LINE	8 LINE	N A	7 LINE	12
P	PARITY	9 LINE	PARTY	8 LINE	13

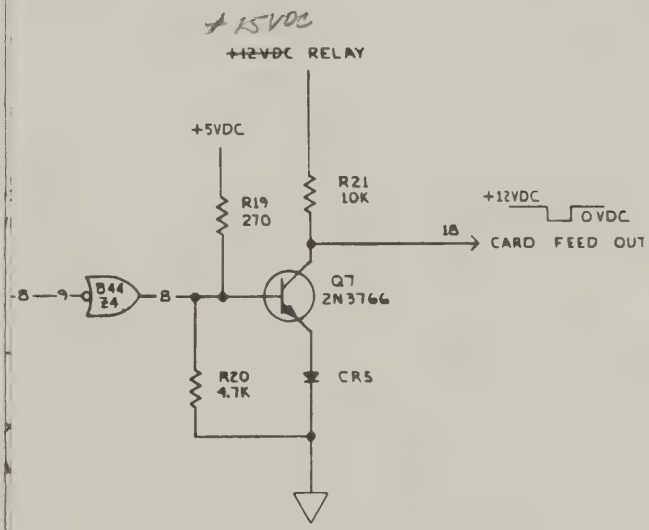
FIGURE 74
INTERFACE DRIVER (PARALLEL)
SCHEMATIC DIAGRAM & COMPONENT LOCATION

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS ±10%, 1/2W.
   B. ALL CAPACITORS ARE IN μF.
   C. ALL DIODES ARE IN4001.
   D. ALL WAVE FORMS ARE 5VP-P (0VDC TO +5VDC)
2. POSITIVE LOGIC USED
3. JUMPERS TO BE INSTALLED DURING ASSEMBLY.
4. →1, →A INDICATE CONNECTOR PIN NUMBERS.



CARD FEED SOLENOID DRIVER

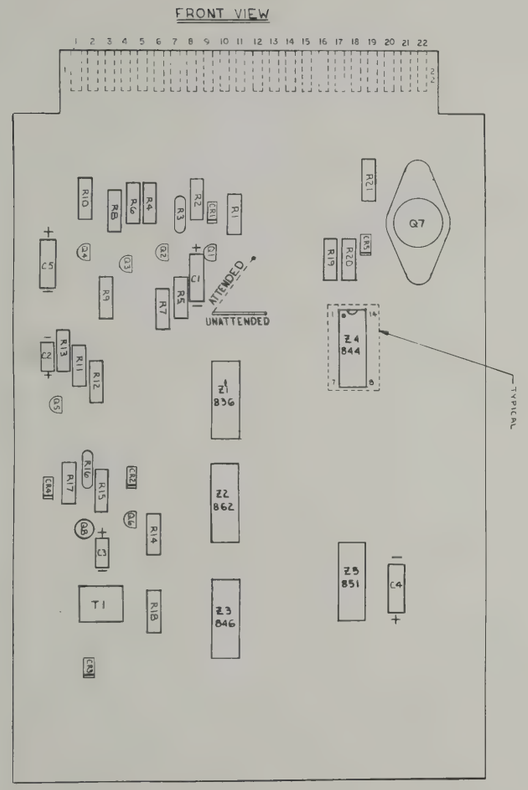


75

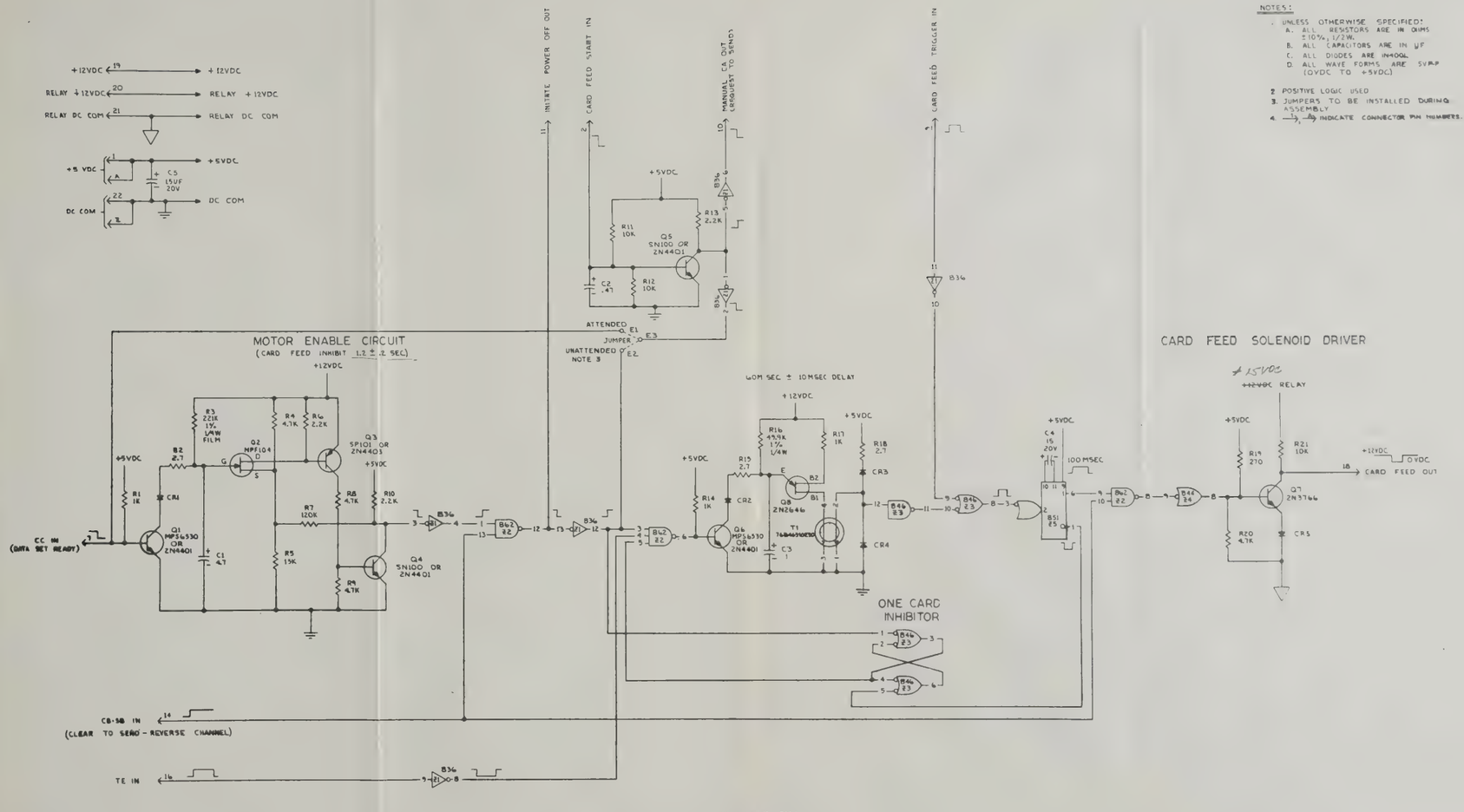
OGIC

ATIC DIAGRAM & COMPONENT LOCATION

D OR UNATTENED



(DWG. NO. 01CF7884G)



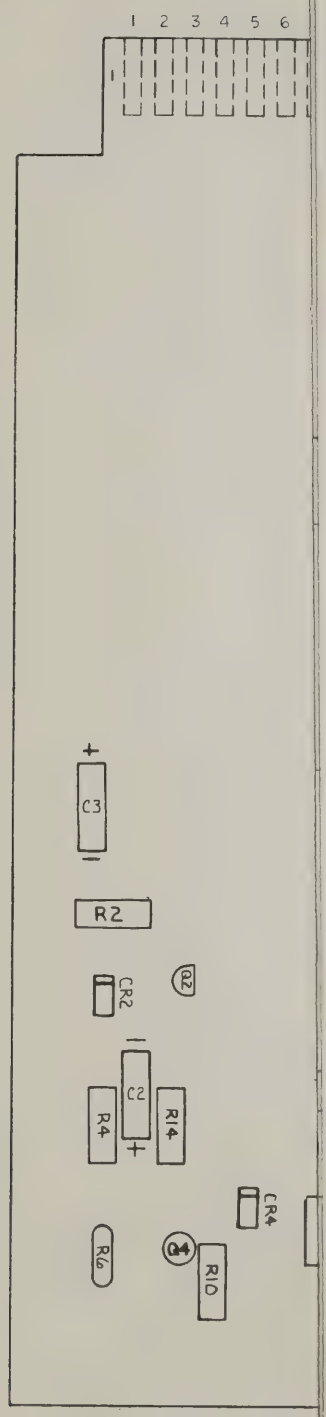
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS ±10%, 1/2W.
   B. ALL CAPACITORS ARE IN μF
   C. ALL DIODES ARE IN4004.
   D. ALL WAVE FORMS ARE 5V P-P (0VDC TO +5VDC)
2. POSITIVE LOGIC USED
3. JUMPERS TO BE INSTALLED DURING ASSEMBLY
4. 1, 2, 3, ETC. INDICATE CONNECTOR PIN NUMBERS.

(DWG. NO. 63DF7884G)

FIGURE 75
FEED LOGIC
SCHEMATIC DIAGRAM & COMPONENT LOCATION

NOTES:

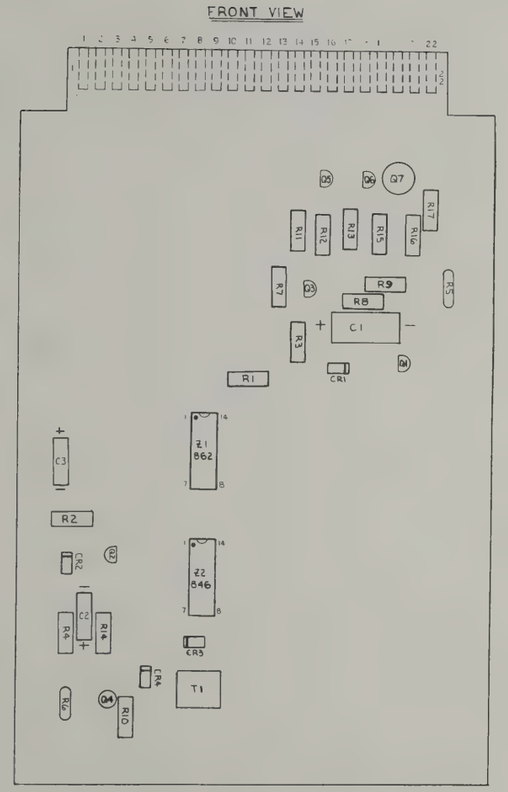
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL WAVE FORMS ARE 5V P-P (OVDC TO +5VDC)
   B. ALL CAPACITORS ARE IN UF.
   C. ALL RESISTORS ARE IN OHMS, ±10 PCT, 1/2W.
   D. ALL DIODES ARE IN4001.
2. POSITIVE LOGIC USED.
3. →1, →A INDICATE CONNECTOR PIN NUMBERS.



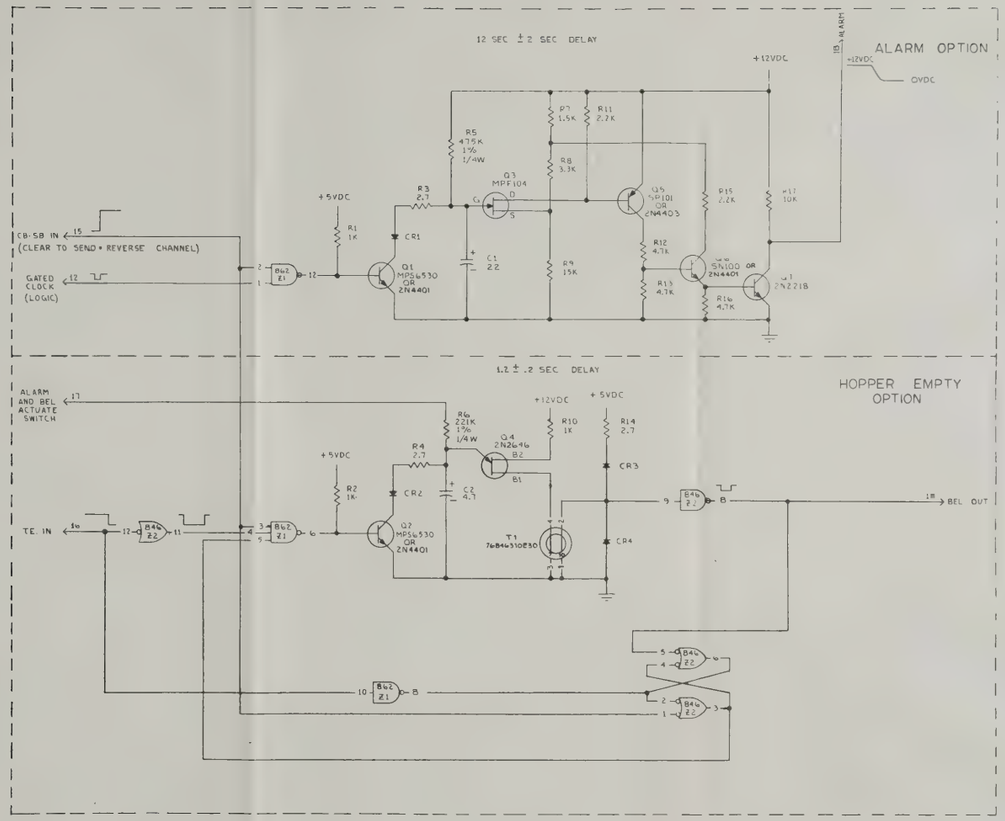
76

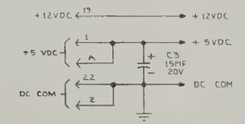
-BEL

ATIC DIAGRAM & COMPONENT LOCATION



(DWG NO. 01CF7886G)



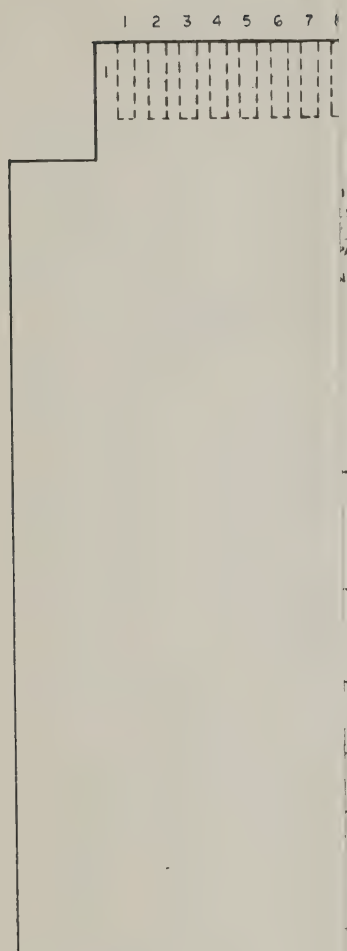


(DWG. NO. 63DF7886G)

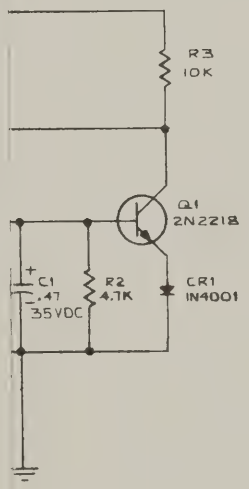
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL WAVE FORMS ARE 5V P-P (0VDC TO +5VDC)
   B. ALL CAPACITORS ARE IN uF
      ALL RESISTORS ARE IN OHMS, ± 10 PCT, ¼ W
   D. ALL DIODES ARE IN4001
2. POSITIVE LOGIC USED
3. ⏚, ⏚ INDICATE CONNECTOR PIN NUMBERS

FIGURE 76
ALARM-BEL
SCHEMATIC DIAGRAM & COMPONENT LOCATION

FR



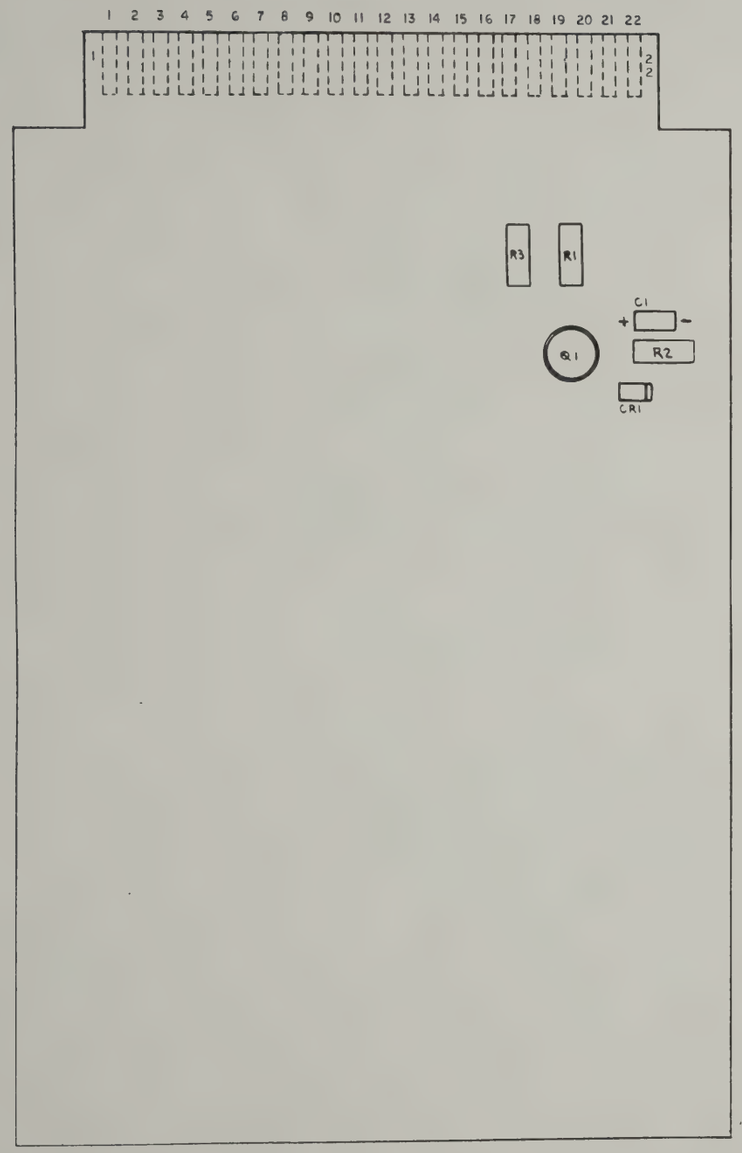
ISE SPECIFIED :
SISTORS ARE IN OHMS
, 1/2 WATT.
PACITORS ARE IN UF.
NNECTOR PIN NUMBERS.



(DWG. NO. 63BF7888G)

C 77
R EMPTY ALARM
ATIC DIAGRAM & COMPONENT LOCATION

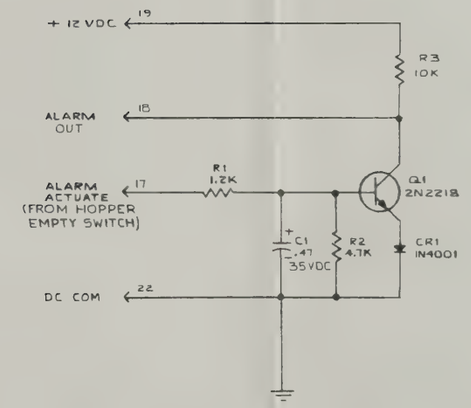
FRONT VIEW



(DWG. NO. 01CF7888G)

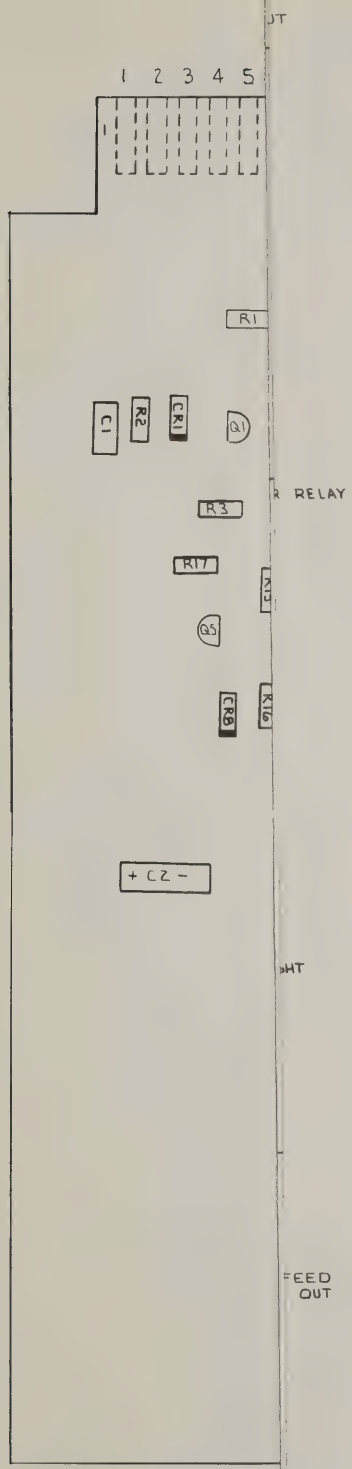
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A. ALL RESISTORS ARE IN OHMS ± 10 PCT, 1/2 WATT.
   - B. ALL CAPACITORS ARE IN UF.
2. 17 → INDICATES CONNECTOR PIN NUMBERS.



(DWG. NO. 63BF7888G)

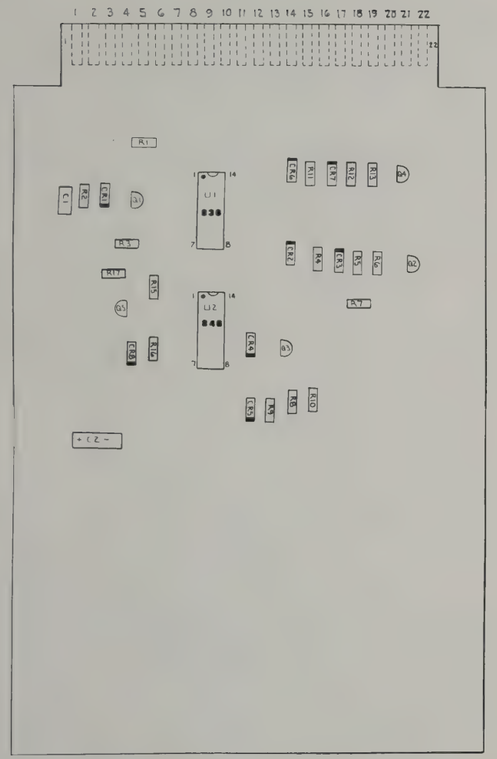
FIGURE 77
HOPPER EMPTY ALARM
SCHEMATIC DIAGRAM & COMPONENT LOCATION



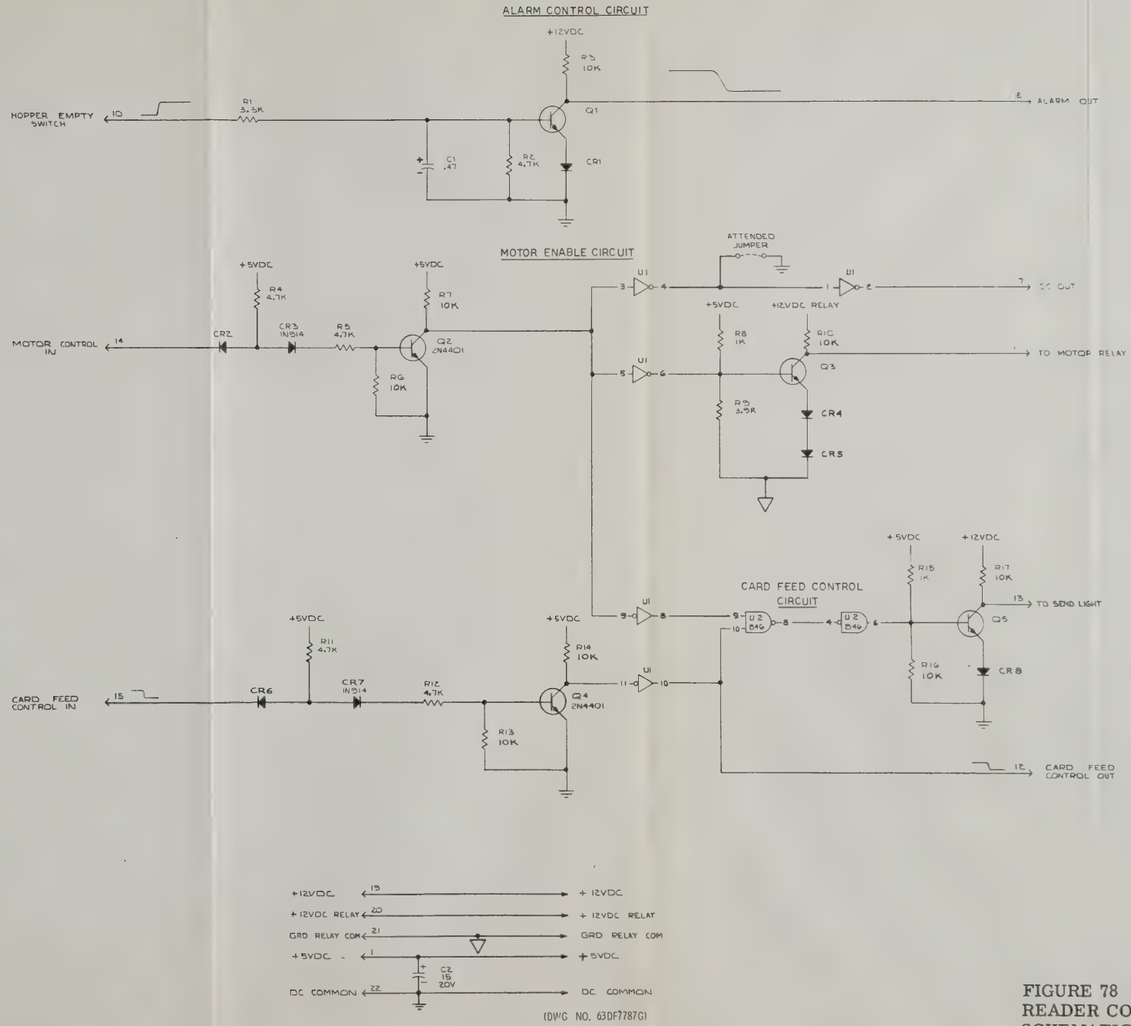
78

R CONTROL INTERFACE (PARALLEL)

ATIC DIAGRAM & COMPONENT LOCATION

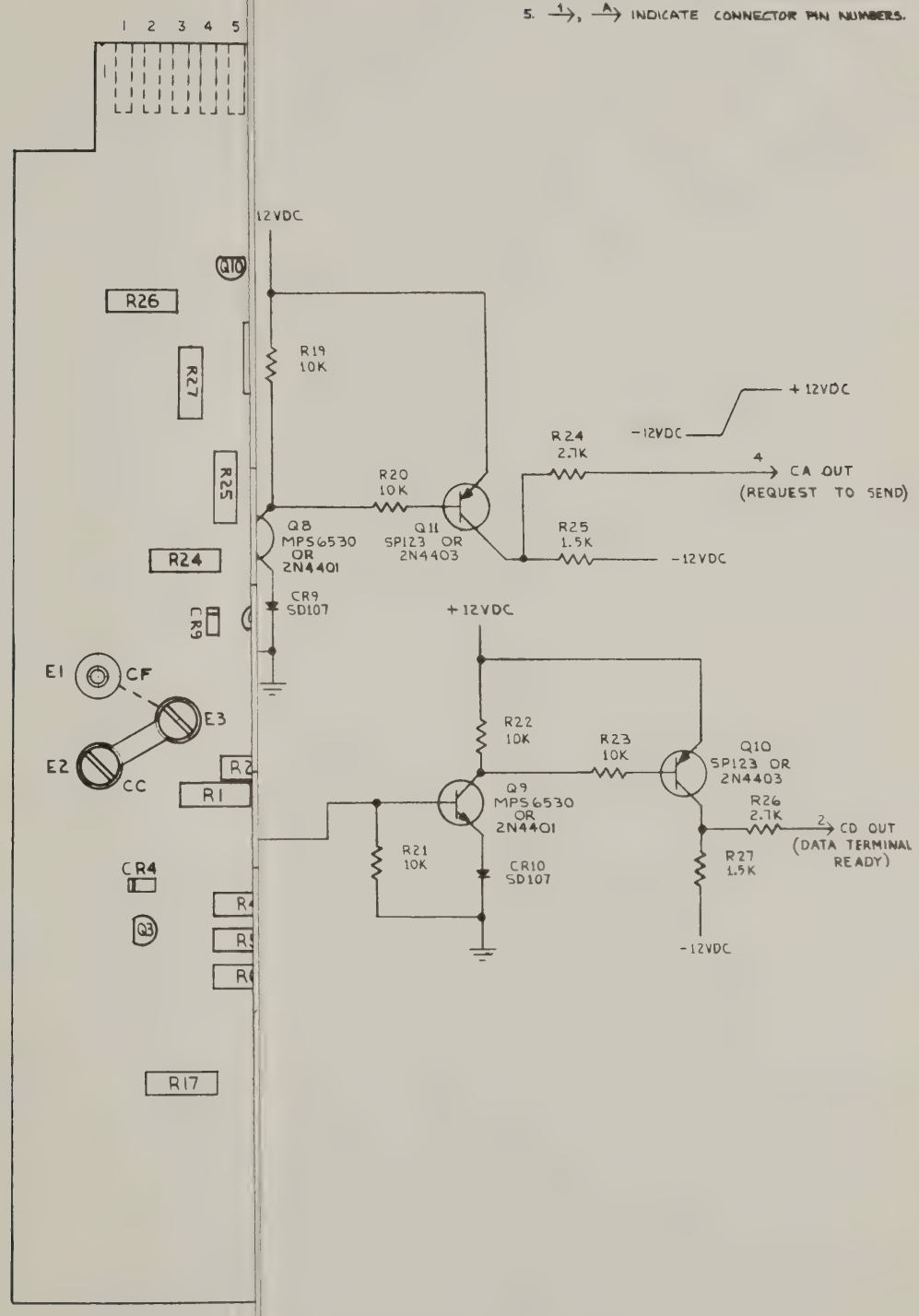


(DWG. NO. 01CF7787G)



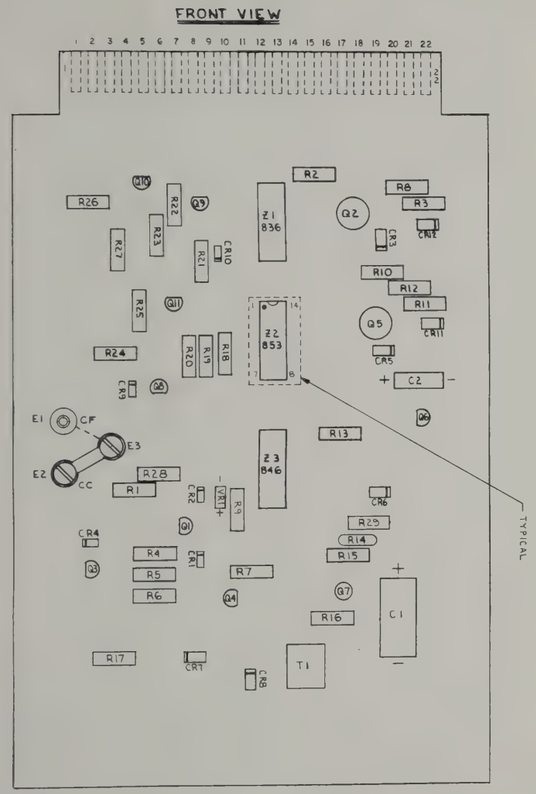
(DWG NO. 63DF7787G)

FIGURE 78
READER CONTROL INTERFACE (PARALLEL)
SCHEMATIC DIAGRAM & COMPONENT LOCATION



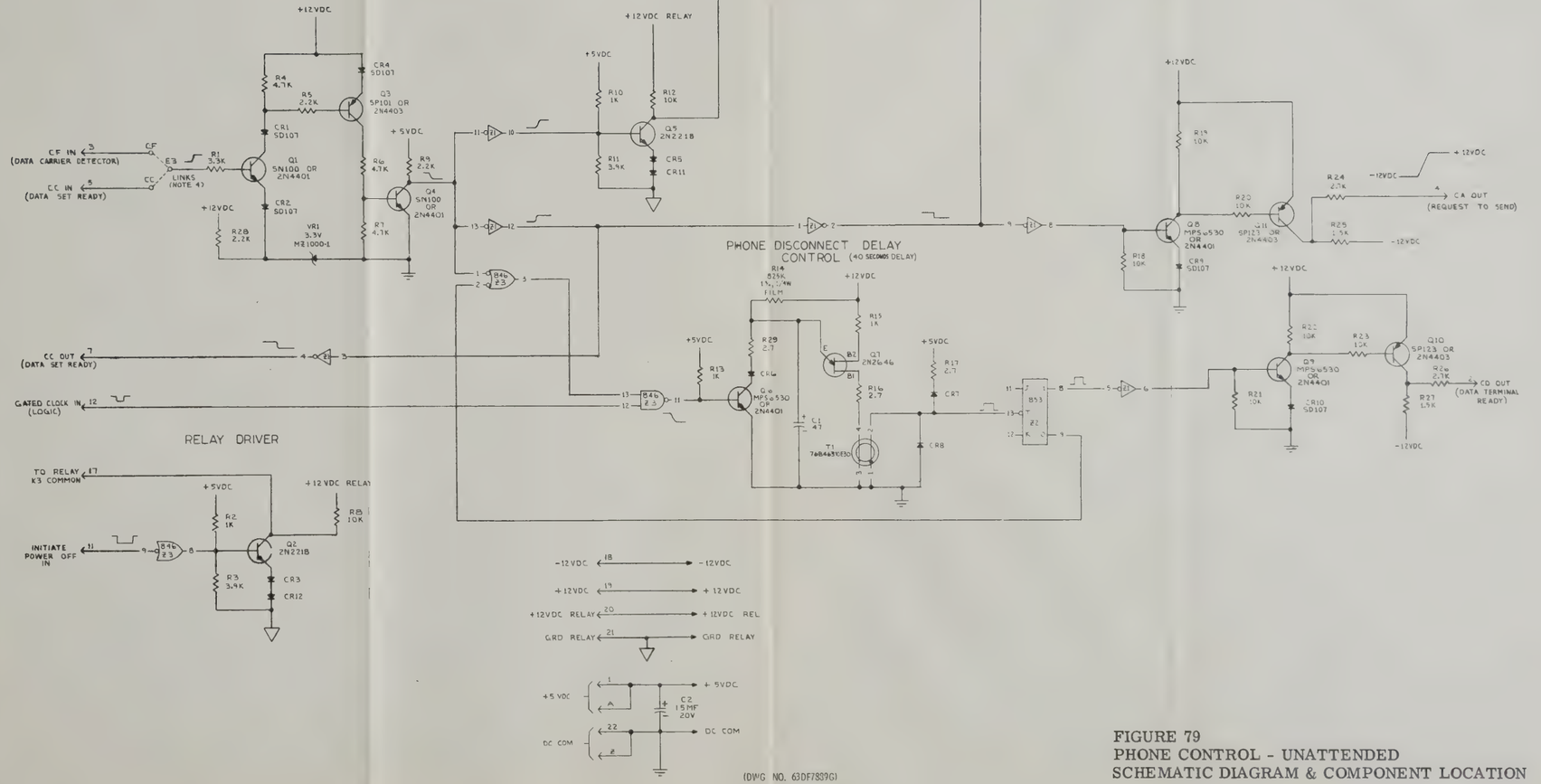
CONTROL - UNATTENDED

ATIC DIAGRAM & COMPONENT LOCATION



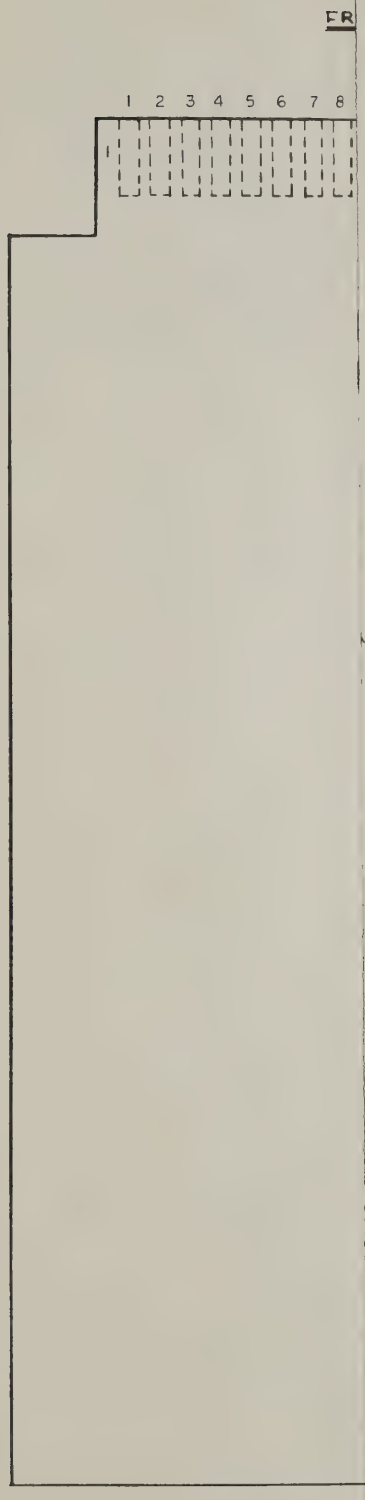
(DWG NO. 01CF7889G)

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS ± 10 PCT 1/2 W.
   B. ALL CAPACITORS ARE IN UF.
   C. ALL DIODES ARE IN4001
   D. ALL WAVE FORMS ARE 5 V P-P (0 VDC TO +5 VDC)
2. POSITIVE LOGIC USED.
3. ALL INVERTERS ARE MC836P
4. LINKS TO BE INSTALLED DURING ASSEMBLY.
5. 1, 2, 3, INDICATE CONNECTOR PIN NUMBERS.



(DWG NO. 63DF7889G)

FIGURE 79
PHONE CONTROL - UNATTENDED
SCHEMATIC DIAGRAM & COMPONENT LOCATION



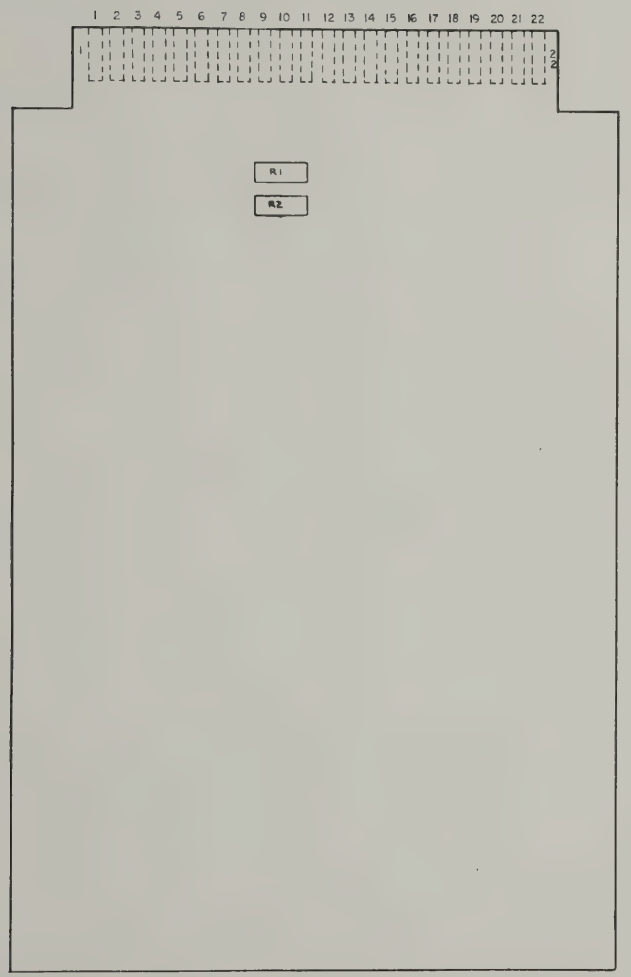
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A ALL RESISTORS ARE IN OHMS ± 10 PCT, 1/2 WATT.
2. 3 → INDICATES CONNECTOR PIN NUMBERS.

(DY)

80
CONTROL - ATTENDED
ATIC DIAGRAM & COMPONENT LOCATION

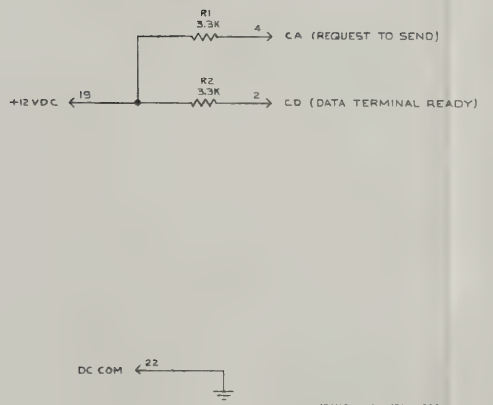
FRONT VIEW



(DWG. NO. 01CF7890G)

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A ALL RESISTORS ARE IN OHMS ±10 PCT, 1/2 WATT
2. 5 → INDICATES CONNECTOR PIN NUMBERS.



(DWG NO. 63BF7890G)

FIGURE 80
PHONE CONTROL - ATTENDED
SCHEMATIC DIAGRAM & COMPONENT LOCATION

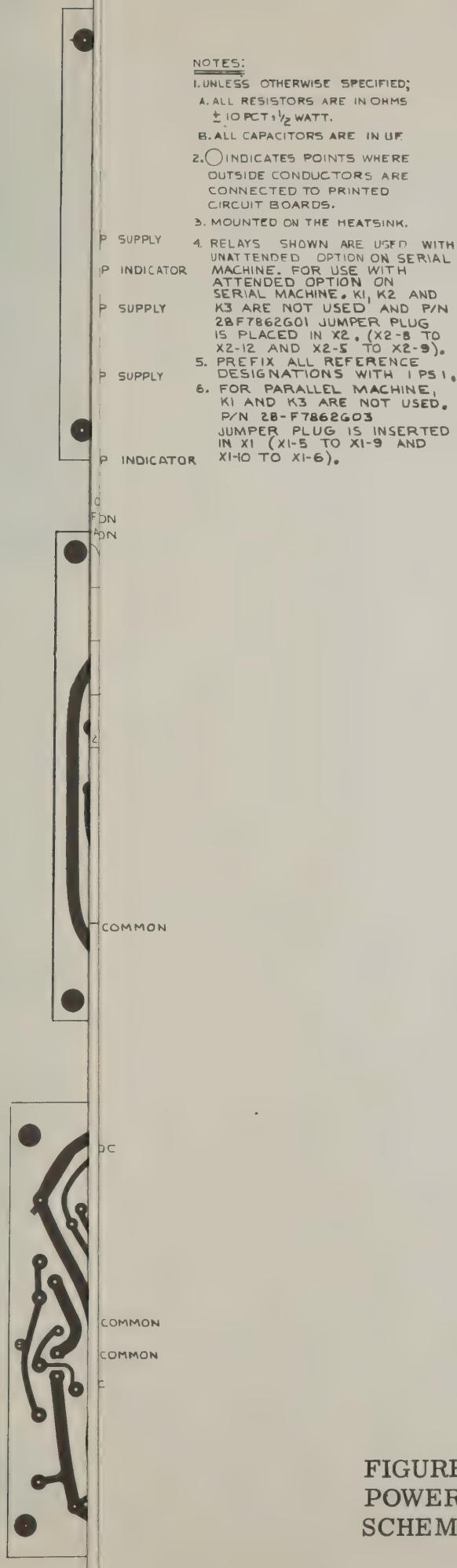
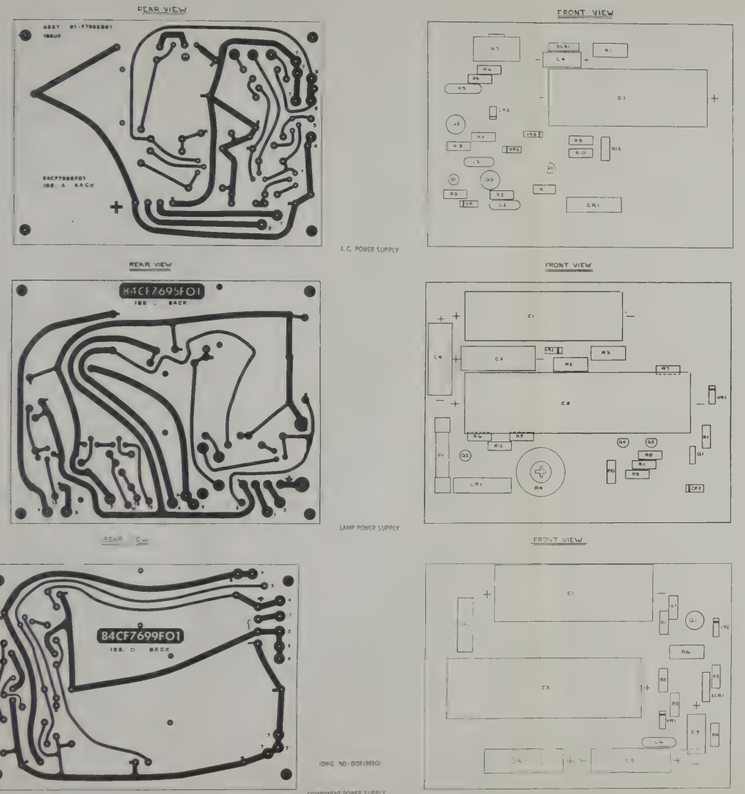

NOTES:
1. UNLESS OTHERWISE SPECIFIED;
A. ALL RESISTORS ARE IN OHMS ± 10 PCT, 1/2 WATT.
B. ALL CAPACITORS ARE IN UF.
2. ◯ INDICATES POINTS WHERE OUTSIDE CONDUCTORS ARE CONNECTED TO PRINTED CIRCUIT BOARDS.
3. MOUNTED ON THE HEATSINK.
4. RELAYS SHOWN ARE USED WITH UNATTENDED OPTION ON SERIAL MACHINE. FOR USE WITH ATTENDED OPTION ON SERIAL MACHINE, K1, K2 AND K3 ARE NOT USED AND P/N 28F7862G01 JUMPER PLUG IS PLACED IN X2, (X2-8 TO X2-12 AND X2-5 TO X2-9).
5. PREFIX ALL REFERENCE DESIGNATIONS WITH 1PS1,
6. FOR PARALLEL MACHINE, K1 AND K3 ARE NOT USED. P/N 28-F7862G03 JUMPER PLUG IS INSERTED IN X1 (X1-5 TO X1-9 AND X1-10 TO X1-6).
P SUPPLY
P INDICATOR
P SUPPLY
P SUPPLY
P INDICATOR
FDN
ADN
COMMON
DC
COMMON
COMMON

FIGURE 81
POWER SUPPLY (LAMP, I. C. & COMPONENT)
SCHEMATIC DIAGRAM & COMPONENT LOCATION



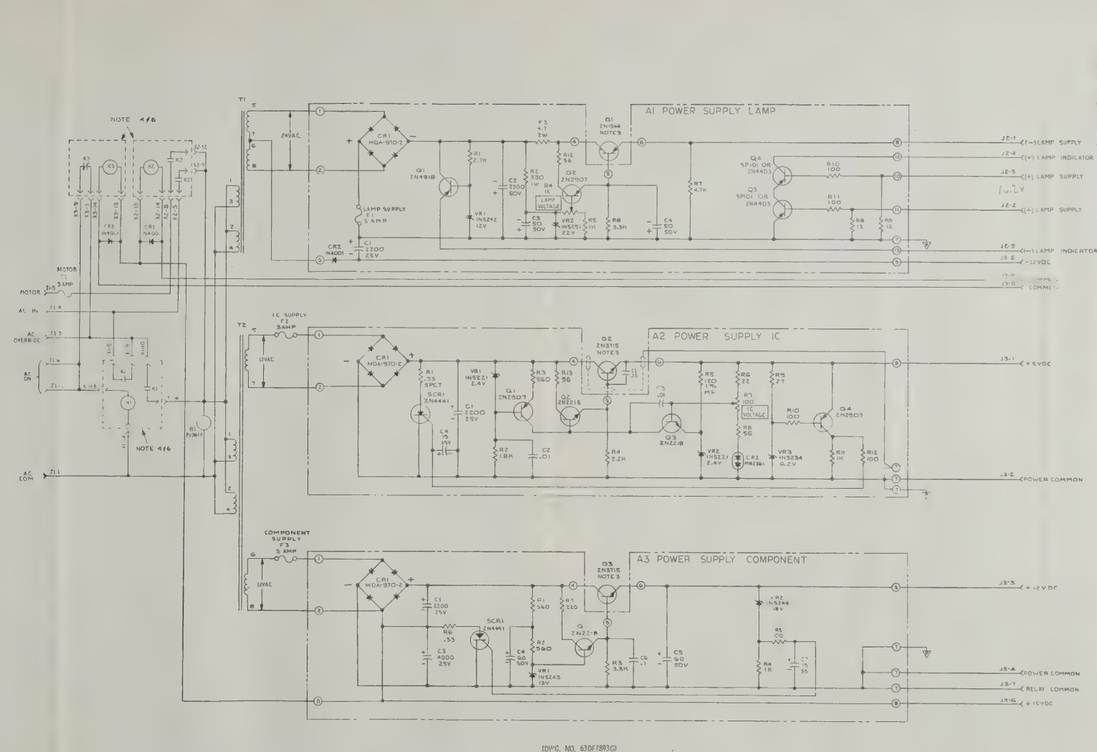


FIGURE 81
POWER SUPPLY (LAMP, I. C. & COMPONENT)
SCHEMATIC DIAGRAM & COMPONENT LOCATION

MDR-1000

LOW-SPEED
DATA TERMINAL
(DATA SET INTERFACE)

The Motorola MDR-1000 Series Document Readers read pencil-marked, key-punched, and preprinted data (or any combination of the three) entered on standard or elongated tab cards, on forms, or on page-size documents of any length.

Optically read data is translated into a standard business machine language, and then transmitted via a local modem to a wide variety of receivers at a remote location. Modems may be data sets, acoustic couplers, or equivalents. Receivers may be teletypewriter sets, paper tape punches, magnetic tape units, card punches, or computers.

The MDR-1000 readers are available for either an attended or unattended operational mode. Unattended Units automatically generate and transmit a BEL code when the hopper is empty, and then initiate an automatic power shutdown at the end of the data transmission.

All MDR-1000 Series Document Readers are supplied with: Interface Cable (9-foot cable terminated at each end with a Cinch or Cannon DBM-25P plug), Card Catcher, Power Cord (6-foot, 3-prong plug), Dust Cover, Operator's Manual, and Deck of Test Cards.

TYPICAL MODELS

MDR-1110C

- *Attended operation*
- *Manual feed only*
- *USASCII alphanumeric output*

MDR-1141C

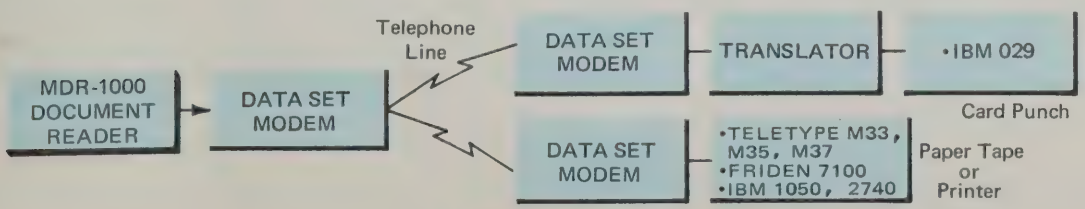
- *Attended operation*
- *Manual or automatic feed with card ejection feature*
- *USASCII numeric output*

MDR-1040C

- *Unattended operation*
- *Manual or automatic feed with card ejection feature*
- *USASCII alphanumeric output*

APPLICATIONS for MDR-1000 Series Document Readers include:

- *Time Sharing*
- *Payroll Records*
- *Production Test Records*
- *Inventory Control*
- *Doctor/Hospital Record Processing*
- *Service Reporting*
- *Utility Reading and Billing Systems*
- *Computer Programming*



System Block Diagram

MOTOROLA
Information Systems

MDR-1000

LOW-SPEED
DATA TERMINAL
(DATA SET INTERFACE)

The Motorola MDR-1000 Series Document Readers read pencil-marked, key-punched, and preprinted data (or any combination of the three) entered on standard or elongated tab cards, on forms, or on page-size documents of any length.

Optically read data is translated into a standard business machine language, and then transmitted via a local modem to a wide variety of receivers at a remote location. Modems may be data sets, acoustic couplers, or equivalents. Receivers may be teletypewriter sets, paper tape punches, magnetic tape units, card punches, or computers.

The MDR-1000 readers are available for either an attended or unattended operational mode. Unattended Units automatically generate and transmit a BEL code when the hopper is empty, and then initiate an automatic power shutdown at the end of the data transmission.

All MDR-1000 Series Document Readers are supplied with: Interface Cable (9-foot cable terminated at each end with a Cinch or Cannon DBM-25P plug), Card Catcher, Power Cord (6-foot, 3-prong plug), Dust Cover, Operator's Manual, and Deck of Test Cards.

TYPICAL MODELS

MDR-1110C

- *Attended operation*
- *Manual feed only*
- *USASCII alphanumeric output*

MDR-1141C

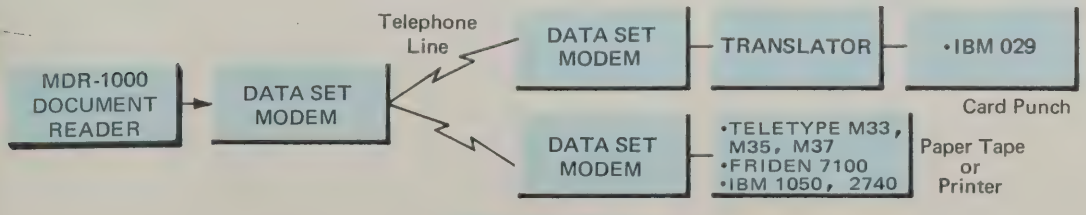
- *Attended operation*
- *Manual or automatic feed with card ejection feature*
- *USASCII numeric output*

MDR-1040C

- *Unattended operation*
- *Manual or automatic feed with card ejection feature*
- *USASCII alphanumeric output*

APPLICATIONS for MDR-1000 Series Document Readers include:

- *Time Sharing*
- *Payroll Records*
- *Production Test Records*
- *Inventory Control*
- *Doctor/Hospital Record Processing*
- *Service Reporting*
- *Utility Reading and Billing Systems*
- *Computer Programming*

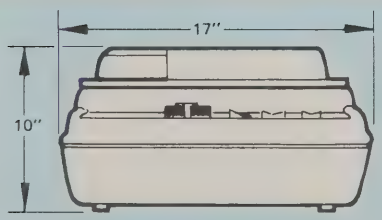


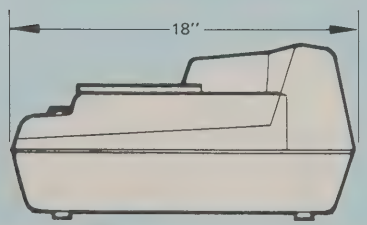
System Block Diagram

MOTOROLA
Information Systems

SPECIFICATIONS

INPUT LANGUAGE	Hollerith code
OUTPUT LANGUAGE	USASCII alphanumeric code (85 characters) USASCII numeric code (11 characters) – optional PTTC/BCD code (72 characters) – optional EBCDIC code (159 characters) – optional
PARITY	Odd, even, or none – at user's option
TRANSMISSION RATE	110 bits/second (10 characters/second scan rate)
COMMUNICATIONS INTERFACE	Conforms to EIA Standard RS-232B for common carrier data transmission equipment
FEED	Manual (tab cards or page-size documents) Optional – automatic hopper feed (includes 250-tab card capacity hopper and card weight)
READING RATE	40-column card . . . . .Minimum -- 8 cards/minute; maximum -- 16 cards/minute using card ejection feature 80-column card . . . . .Minimum -- 4 cards/minute; maximum -- 8 cards/minute using card ejection feature
AUTOMATIC END-OF-DATA CARD EJECTION	Increases card thruput -- included on automatic feed models
CONTROL CODES	Two leading-edge codes and one trailing-edge code generated as document enters and exits read head. Ten control codes available for selection (only four codes when using USASCII numeric output)
ALARMS	Audible and visual alarms provided to indicate "Hopper Empty" and "Card Jam" conditions -- included on automatic feed models
POWER REQUIREMENTS	117 Vac±10%, 50-60 Hz, 1.5 A
ENVIRONMENTAL CONDITIONS	(Applies only to Document Reader; not to modems or documents) Temperature . . . . . 40°F to 120°F (operating and storage) Relative Humidity. . . . . 10% to 95%





PHYSICIAL CHARACTERISTICS

HEIGHT.....10 inches
WIDTH .....17 inches (less card catcher)
24 inches (with card catcher)
DEPTH .....18 inches
WEIGHT.....45 pounds
COLOR .....Beige

For further information, call or write:

MOTOROLA Instrumentation and Control Inc.
A SUBSIDIARY OF MOTOROLA INC.
P. O. BOX 5409 • PHOENIX, ARIZONA 85010 • PHONE (602) 959-1000

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MDR-2000

HIGH-SPEED
DATA TERMINAL

The Motorola MDR-2000 Series Document Readers read pencil-marked, key-punched, and preprinted data (or any combination of the three) entered on standard or elongated tab cards, on forms, or on page-size documents of any length.

Optically read data is translated into a standard business machine language, and then transmitted via a local modem to a wide variety of receivers at a remote location. Modems may be data sets, or equivalents. Receivers may be teletypewriter sets, paper tape punches, magnetic tape units, or computers.

The MDR-2000 Readers are available for either attended or unattended operational mode. Unattended units automatically generate and transmit a BEL code when the hopper is empty, and then initiate an automatic power shutdown at the end of the data transmission.

All MDR-2000 Document Readers are supplied with: Interface Cable (9-foot cable terminated at each end with a Cinch or Cannon DBM-25P plug), Card Catcher, Power Cord (6-foot, 3-prong plug), Dust Cover, Operator's Manual, and Test Cards.

TYPICAL MODELS

MDR-2110B

- *Attended operation*
- *Manual feed only*
- *USASCII alphanumeric output*

MDR-2141B

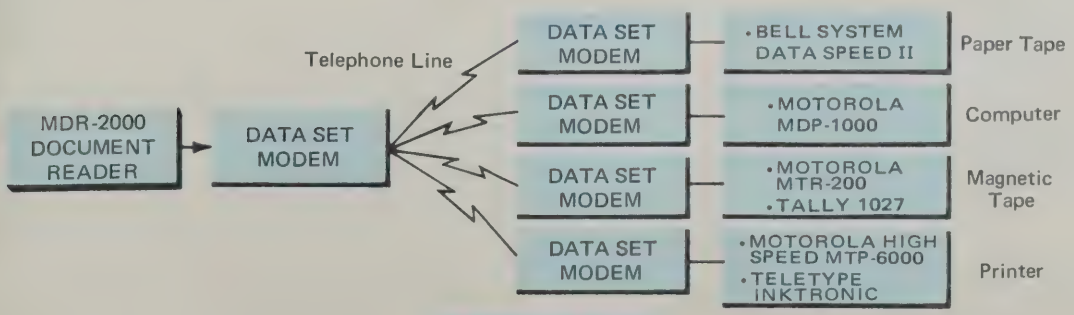
- *Attended operation*
- *Manual or automatic feed with card ejection feature*
- *USASCII numeric output*

MDR-2040B

- *Unattended operation*
- *Manual or automatic feed with card ejection feature*
- *USASCII alphanumeric output*

APPLICATIONS for the MDR-2000 Series Document Readers include:

- *Student Records*
- *Payroll Records*
- *Production Test Records*
- *Doctor/Hospital Record Processing*
- *Service Reporting*
- *Utility Reading and Billing Systems*

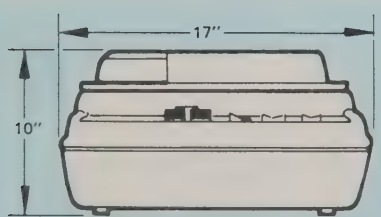


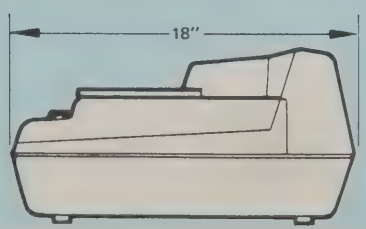
System Block Diagram

MOTOROLA
Information Systems

SPECIFICATIONS

INPUT LANGUAGE	Hollerith code
OUTPUT LANGUAGE	USASCII alphanumeric code (85 characters) USASCII numeric code (11 characters) -- optional PTTC/BCD code (72 characters) -- optional EBCDIC code (159 characters) -- optional
PARITY	Odd, even, or none -- at user's option
TRANSMISSION RATE	1050 bits/second (70 characters/second scan rate)
COMMUNICATIONS INTERFACE	Conforms to EIA Standard RS-232B for common carrier data transmission equipment
FEED	Manual (tab cards or page-size documents) Optional -- automatic hopper feed (includes 250-tab card capacity hopper and card weight)
READING RATE	40-column card . . . . . Minimum -- 60 cards/minute; maximum -- 120 cards/minute using card ejection feature 80-column card . . . . . Minimum -- 30 cards/minute; maximum -- 60 cards/minute using card ejection feature
AUTOMATIC END-OF-DATA CARD EJECTION	Increases card thruput -- included on automatic feed models
CONTROL CODES	Two leading-edge codes and one trailing-edge code generated as document enters and exits read head. Ten control codes available for selection (only four codes when using USASCII numeric output)
SECURITY	Card feed controllable by reverse channel (SB) signal from modem
ALARMS	Audible and visual alarms provided to indicate "Hopper Empty" and "Card Jam" conditions -- included on automatic feed models
POWER REQUIREMENTS	117 Vac±10%, 50-60 Hz, 1.5 A
ENVIRONMENTAL CONDITIONS	(Applies only to Document Reader; not to documents or modems) Temperature . . . . . 40°F to 120°F (operating and storage) Relative Humidity . . . . . 10% to 95%





PHYSICIAL CHARACTERISTICS

HEIGHT. . . . 10 inches
WIDTH . . . . 17 inches (less card catcher)
24 inches (with card catcher)
DEPTH . . . . 18 inches
WEIGHT. . . . 45 pounds
COLOR . . . . Beige

For further information, call or write:

MOTOROLA Instrumentation and Control Inc.
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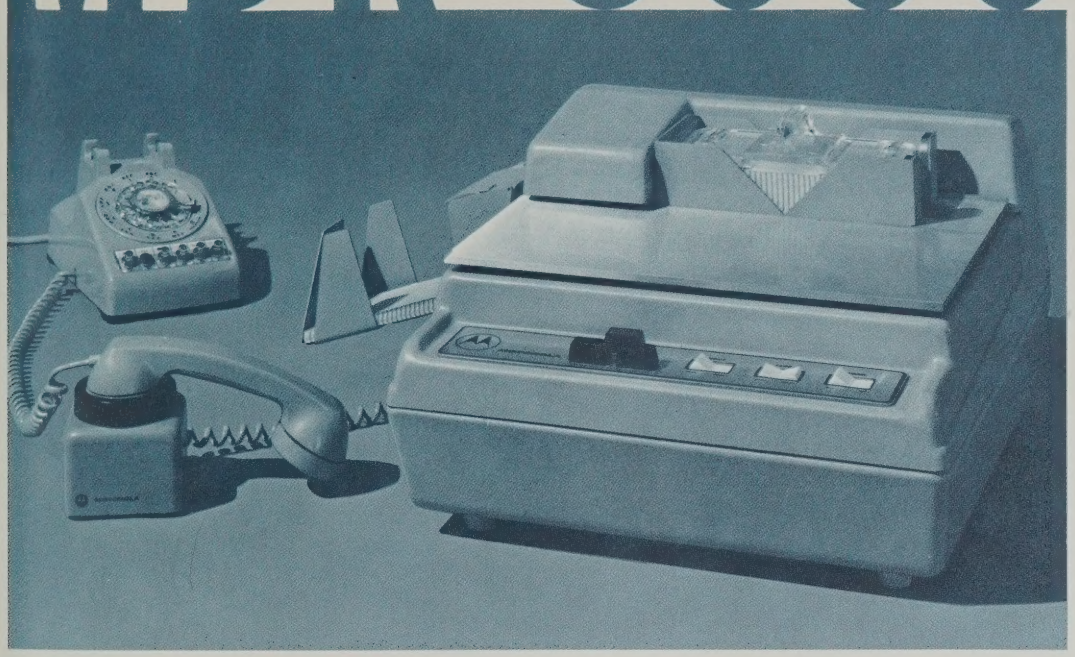
MDR-3000

ACOUSTIC-COUPLED DATA TERMINAL



The Motorola MDR-3000 Series Document Readers read pencil-marked, key-punched, and preprinted data (or any combination of the three) entered on standard or elongated tab cards, on forms, or on page-size documents of any length.

Optically read data is translated into a standard business machine language, and then transmitted via an included Acoustic-Coupled Modem over any standard telephone handset to a wide variety of receivers at a remote location. Receivers may be teletypewriter sets, paper tape punches, magnetic tape units, card punches, or computers.

The integral acoustic-coupled modem of the MDR-3000 allows the reader to be operated as a transportable data transmission terminal.

All MDR-3000 Series Document Readers are supplied with: Acoustic-Coupled Modem, Card Catcher, Power Cord (6-foot, 3-prong plug), Dust Cover, Operator's Manual, and Deck of Test Cards.

TYPICAL MODELS

MDR-3110C

- *Attended operation*
- *Manual feed only*
- *USASCII alphanumeric output*

MDR-3111C

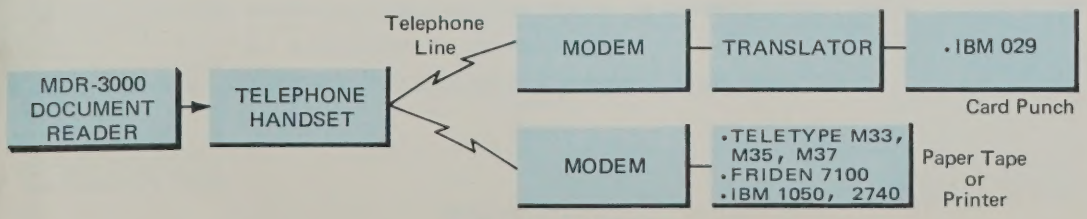
- *Attended operation*
- *Manual feed only*
- *USASCII numeric output*

MDR-3140C

- *Attended operation*
- *Manual or automatic feed with card ejection feature*
- *USASCII alphanumeric output*

APPLICATIONS for the MDR-3000 Series Document Readers include:

- *Consumer Surveys*
- *Time Sharing*
- *Inventory Control*
- *Opinion Polls*
- *Doctor/Hospital Record Processing*
- *Service Reporting*
- *Utility Reading and Billing Systems*
- *Order Entry*

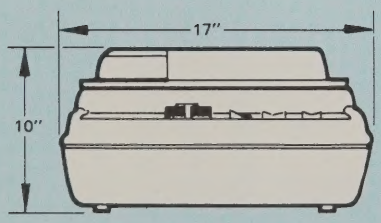


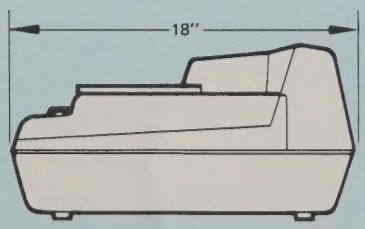
System Block Diagram

MOTOROLA Information Systems

SPECIFICATIONS

INPUT LANGUAGE	Hollerith code
OUTPUT LANGUAGE (Optional)	7-bit output . . . . . PTTC/BCD code (72 characters) 8-bit output . . . . . USASCII alphanumeric code (85 characters) or EBCDIC code (159 characters) 12-bit output . . . . . Hollerith code (no decoding)
PARITY	Odd, even, or none -- at user's option
SCAN RATE (Optional)	10/20 characters/second 70/140 characters/second
INTERFACE CABLING	Maximum distance of 50 feet
FEED	Manual (tab cards or page-size documents) Optional - automatic hopper feed (includes 250-tab card capacity hopper and card weight)
AUTOMATIC END-OF-DATA CARD EJECTION	Increases card thruput -- included on automatic feed models
CONTROL CODES	One leading-edge code and one trailing-edge code generated as document enters and exits read head. Ten control codes available for selection (not available with Hollerith output codes)
ALARMS	Audible and visual alarms provided to indicate "Hopper Empty" condition – included on automatic feed models.
POWER REQUIREMENTS	117 Vac±10%, 50-60 Hz, 1.5 A
ENVIRONMENTAL CONDITIONS	(Applies only to Document Reader; not to documents) Temperature . . . . . 40°F to 120°F (operating and storage) Relative Humidity . . . . . 10% to 95%





PHYSICAL CHARACTERISTICS

HEIGHT	10 inches	**DEPTH**	18 inches
WIDTH	17 inches (less card catcher) 24 inches (with card catcher)	**WEIGHT**	45 pounds
		COLOR	Beige

For further information, call or write:

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MDR-9000

LOW-SPEED
DATA TERMINAL
(DC INTERFACE)

The Motorola MDR-9000 Series Document Readers are attended units that read pencil-marked, keypunched, and preprinted data (or any combination of the three) entered on standard or elongated tab cards, on forms, or on page-size documents of any length.

Optically read data is translated into a standard business machine language, and then transmitted via a local teletypewriter system and modem over telephone lines to a wide variety of receivers at a remote location. Modems may be data sets, acoustic couplers, or equivalents. Receivers may be teletypewriter sets, paper tape punches, magnetic tape units, card punches, or computers.

All MDR-9000 Series Document Readers are supplied with: Teletypewriter Interface Connector (2-point terminal block), Card Catcher, Power Cord (6-foot, 3-prong plug), Dust Cover, Operator's Manual, and Deck of Test Cards.

TYPICAL MODELS

MDR-9210C

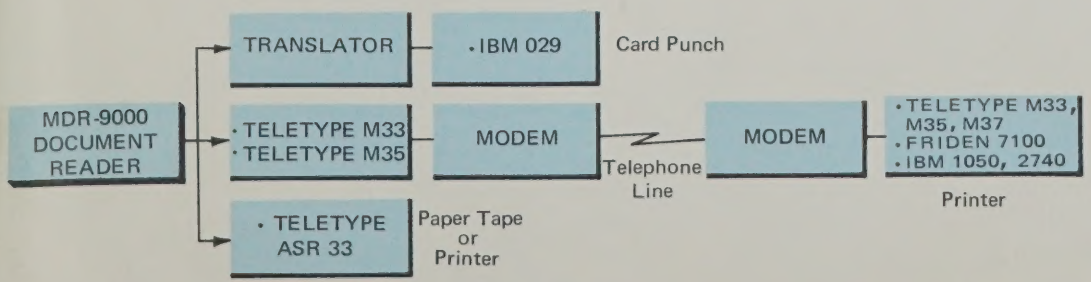
- *Attended operation*
- *Manual feed only*
- *USASCII alphanumeric output*

MDR-9240C

- *Attended operation*
- *Manual or automatic feed with card ejection feature*
- *USASCII alphanumeric output*

APPLICATIONS for the MDR-9000 Series Document Readers include:

- *Parts Inspection*
- *Time Sharing*
- *Payroll Records*
- *Production Test Records*
- *Inventory Control*
- *Library Records*
- *Doctor/Hospital Record Processing*
- *Service Reporting*
- *Utility Reading and Billing Systems*
- *Computer Programming*

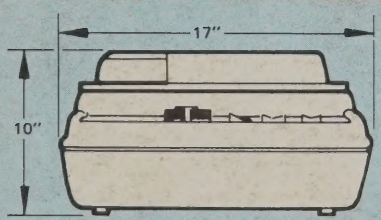


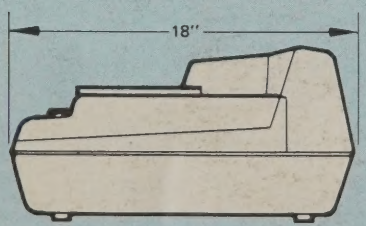
System Block Diagram

MOTOROLA
Information Systems

SPECIFICATIONS

INPUT LANGUAGE	Hollerith code
OUTPUT LANGUAGE	USASCII alphanumeric code (85 characters) USASCII numeric code (11 characters) -- optional PTTC/BCD code (72 characters) -- optional EBCDIC code (159 characters) -- optional
PARITY	Odd, even, or none -- at user's option
TRANSMISSION RATE	110 bits/second (10 characters/second scan rate)
COMMUNICATIONS INTERFACE	Dry contact (applicable in 20 mA or 60 mA dc circuit)
FEED	Manual (tab cards or page-size documents) Optional -- automatic hopper feed (includes 250-tab card capacity hopper and card weight)
READING RATE	40-column card . . . . . Minimum -- 8 cards/minute; maximum -- 16 cards/minute using card ejection feature 80-column card . . . . . Minimum -- 4 cards/minute; maximum -- 8 cards/minute using card ejection feature
AUTOMATIC END-OF-DATA CARD EJECTION	Increases card thruput -- included on automatic feed models
CONTROL CODES	Two leading-edge codes and one trailing-edge code generated as document enters and exits read head. Ten control codes available for selection (only four codes when using USASCII numeric output)
ALARMS	Audible and visual alarms provided to indicate "Hopper Empty" condition -- included on automatic feed models
POWER REQUIREMENTS	117 Vac±10%, 50-60 Hz, 1.5 A
ENVIRONMENTAL CONDITIONS	(Applies only to Document Reader; not to documents or modems) Temperature . . . . . 40°F to 120°F (operating and storage) Relative Humidity . . . . . 10% to 95%





PHYSICIAL CHARACTERISTICS

HEIGHT. . . . 10 inches
WIDTH . . . . 17 inches (less card catcher)
24 inches (with card catcher)
DEPTH . . . . 18 inches
WEIGHT. . . . 45 pounds
COLOR . . . . Beige

For further information call or write:

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